FIG.1

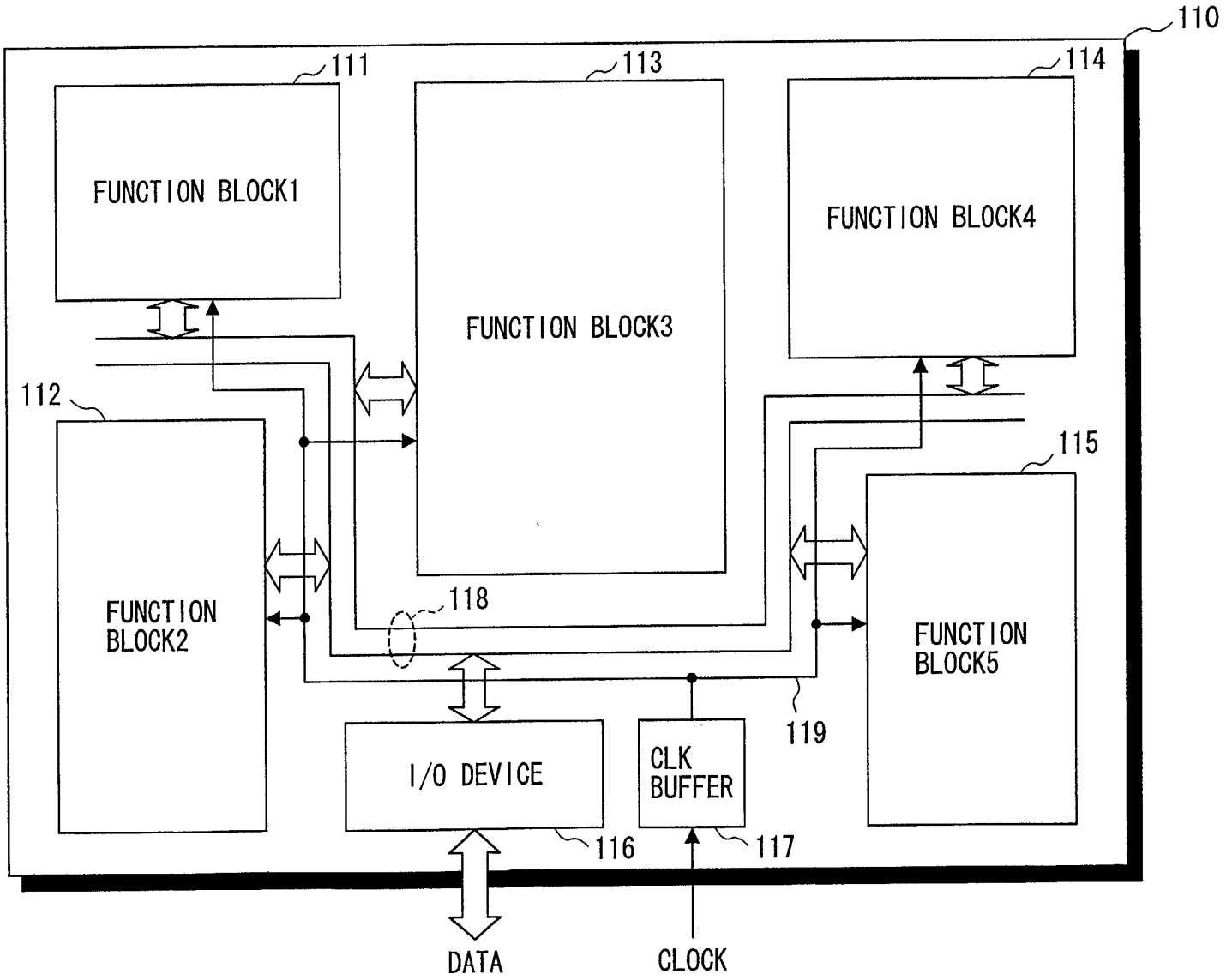

110
111
113
114
FUNCTION BLOCK1
FUNCTION BLOCK3
FUNCTION BLOCK4
112
115
FUNCTION BLOCK2
118
FUNCTION BLOCK5
119
I/O DEVICE
CLK BUFFER
116
117
DATA
CLOCK

FIG.2

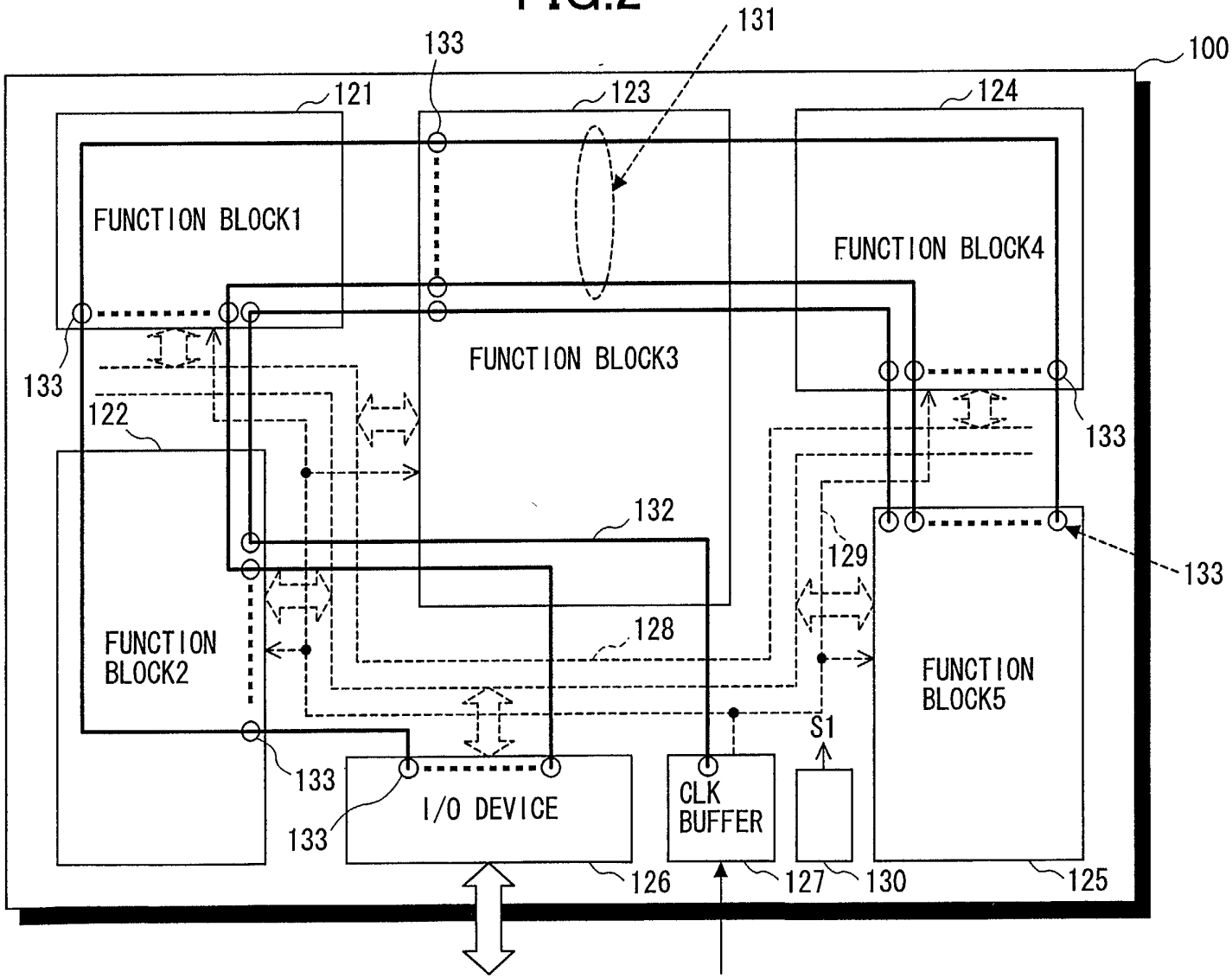

100
131
133
121
123
124
FUNCTION BLOCK1
FUNCTION BLOCK4
FUNCTION BLOCK3
133
122
133
132
129
133
128
FUNCTION BLOCK2
FUNCTION BLOCK5
S1
133
133
I/O DEVICE
CLK BUFFER
126
127
130
125

FIG. 3

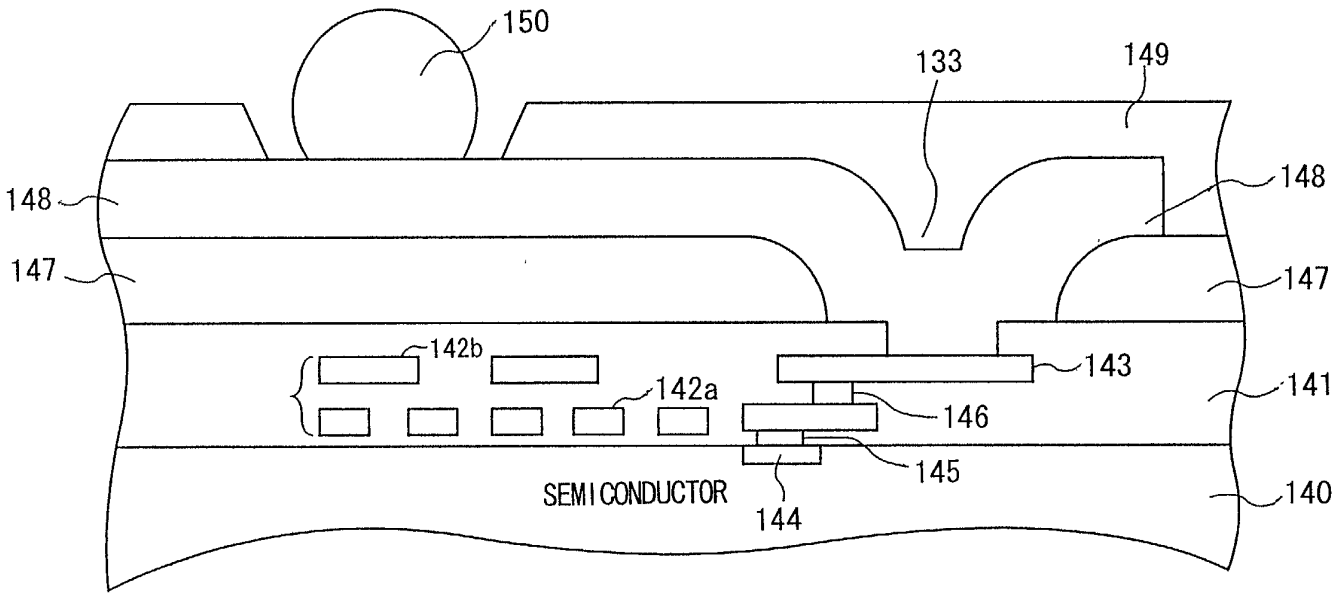

150
133
149
148
148
147
147
142b
143
142a
141
146
145
SEMICONDUCTOR
144
140

FIG.4

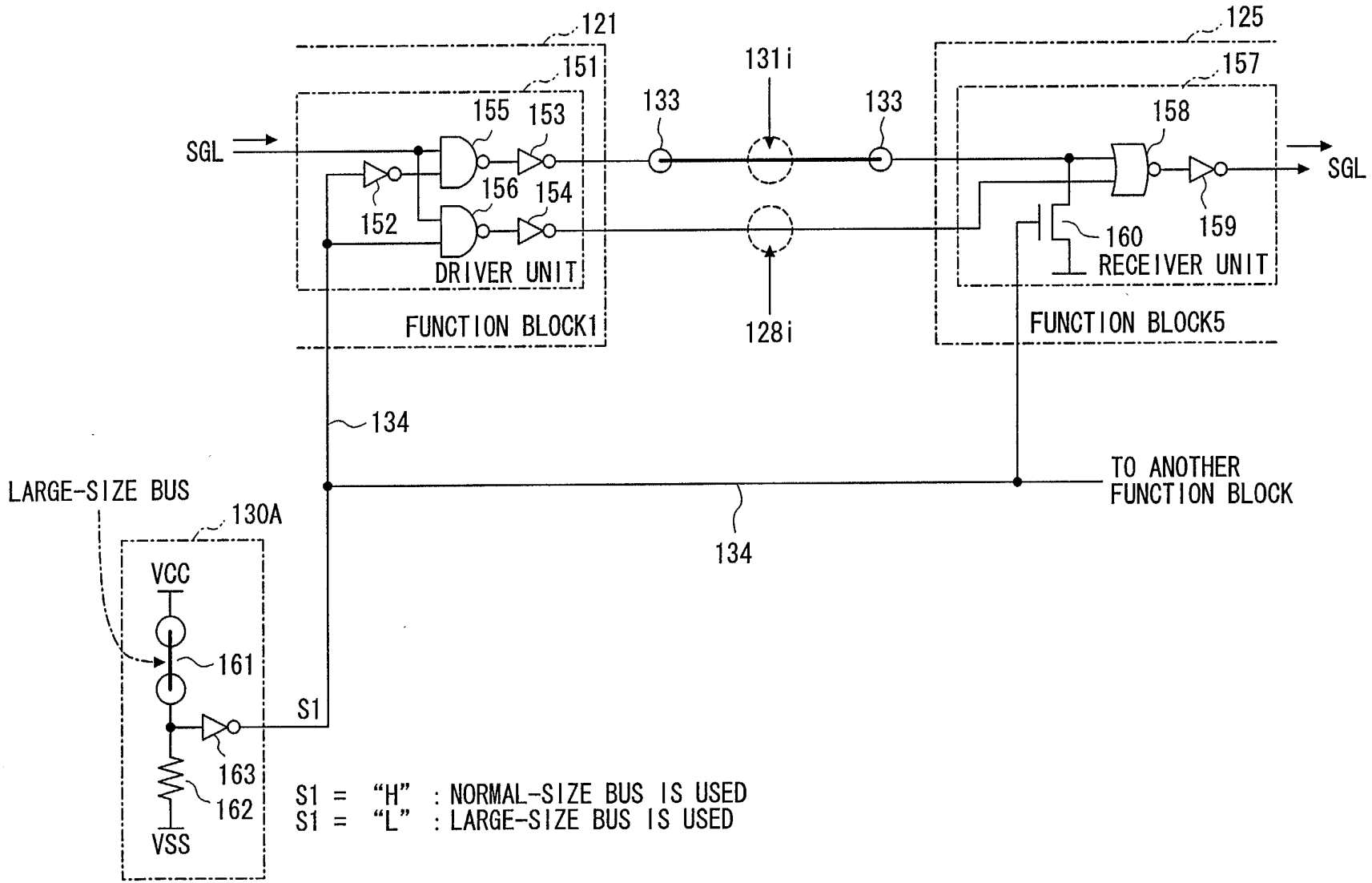

121
151
155
153
133
131i
133
125
157
158
SGL
156
154
152
160
159
SGL
DRIVER UNIT
RECEIVER UNIT
FUNCTION BLOCK1
128i
FUNCTION BLOCK5
134
LARGE-SIZE BUS
TO ANOTHER
FUNCTION BLOCK
130A
134
VCC
161
S1
163
162
VSS
S1 = "H" : NORMAL-SIZE BUS IS USED
S1 = "L" : LARGE-SIZE BUS IS USED

FIG.5

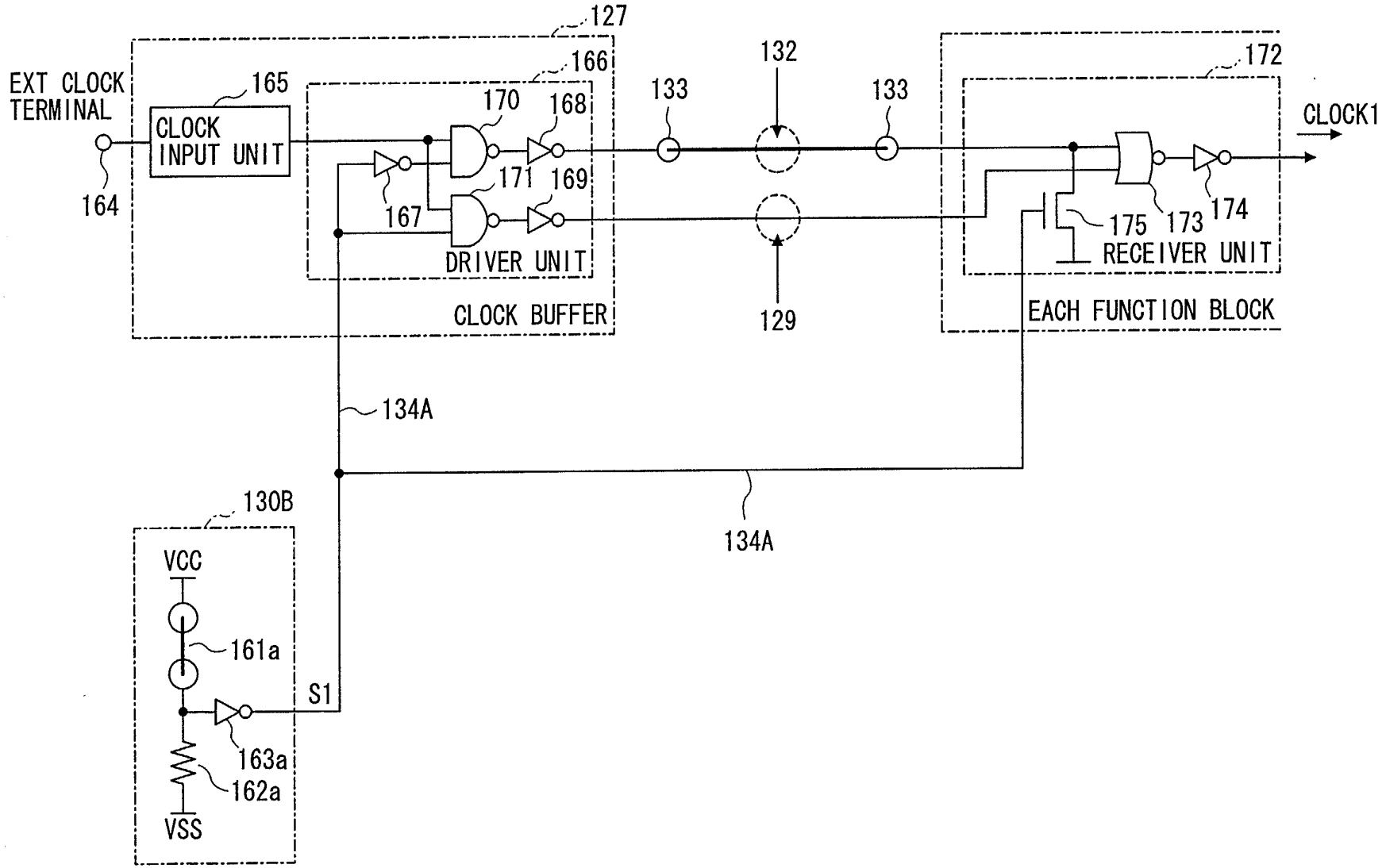

127
166
EXT CLOCK TERMINAL
165
CLOCK INPUT UNIT
164
170
168
171
169
167
DRIVER UNIT
CLOCK BUFFER
133
132
133
129
172
CLOCK1
175
173
174
RECEIVER UNIT
EACH FUNCTION BLOCK
134A
134A
130B
VCC
161a
S1
163a
162a
VSS

FIG.6

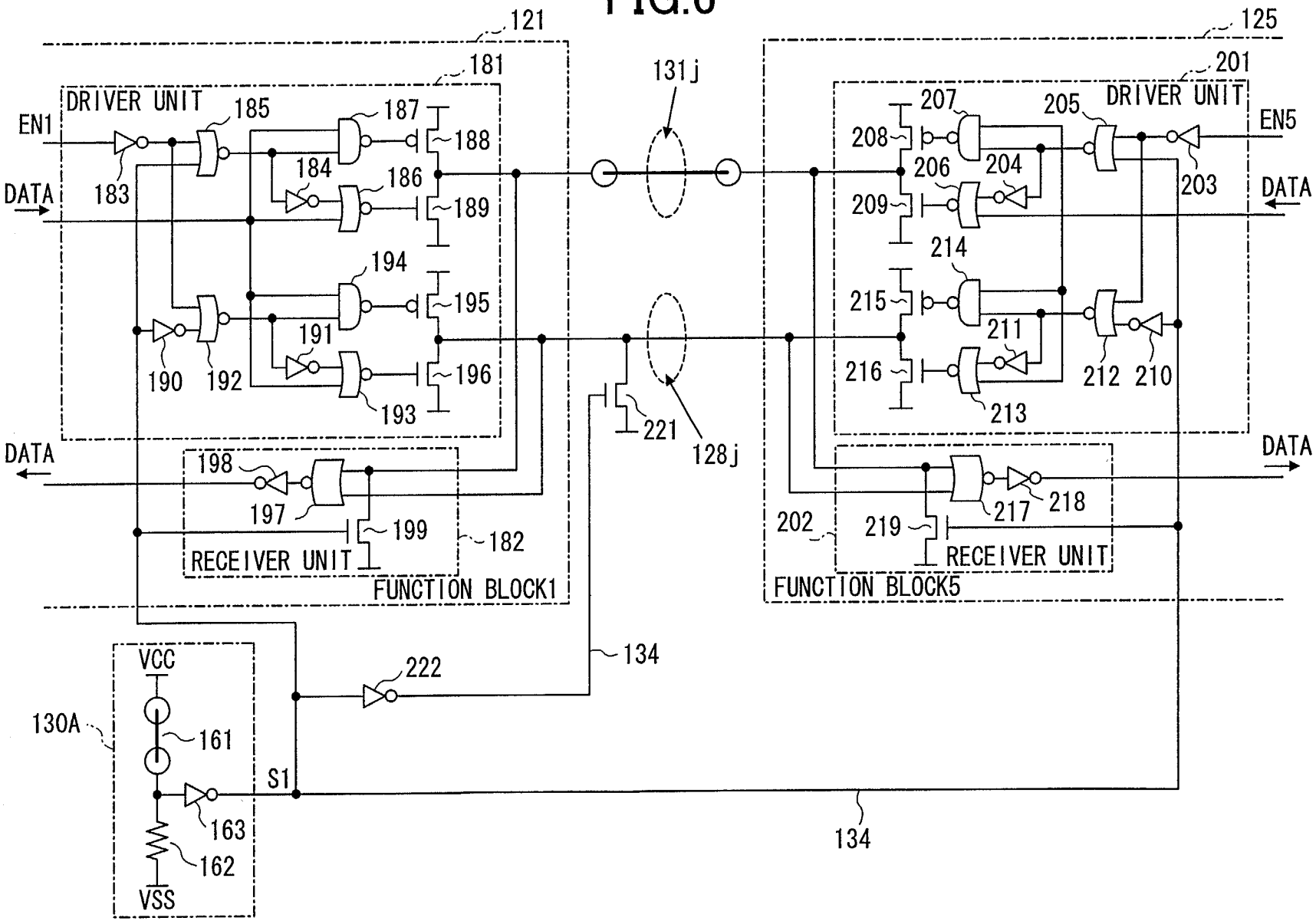

121
125
181
201
131j
DRIVER UNIT
DRIVER UNIT
EN1
EN5
DATA
DATA
183
185
187
188
184
186
189
194
195
191
196
190
192
193
207
205
208
206
204
203
209
214
215
211
216
212
210
213
221
128j
198
197
199
182
RECEIVER UNIT
FUNCTION BLOCK1
202
217
218
219
RECEIVER UNIT
FUNCTION BLOCK5
134
222
VCC
130A
161
S1
163
162
VSS
134

FIG.7A

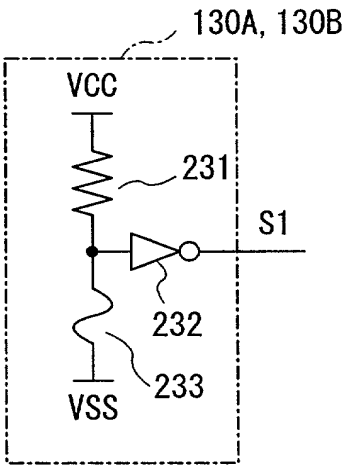


FIG.7B

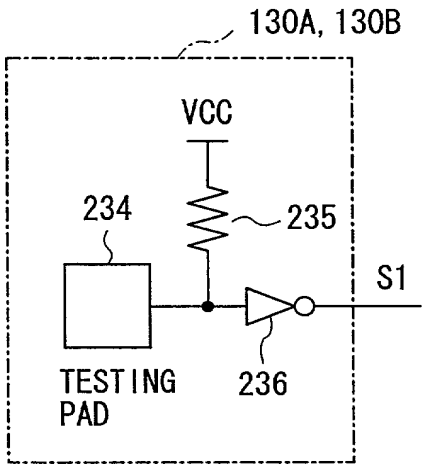


FIG.7C

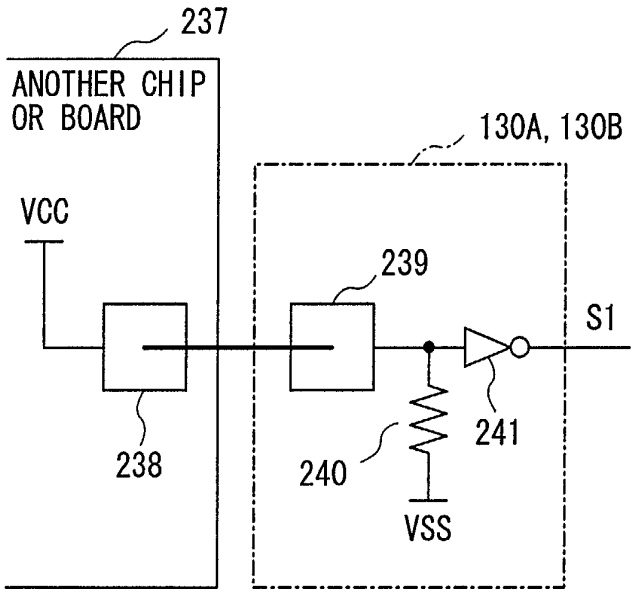

237
ANOTHER CHIP
OR BOARD
130A, 130B
VCC
239
S1
238
240
241
VSS

FIG.7D

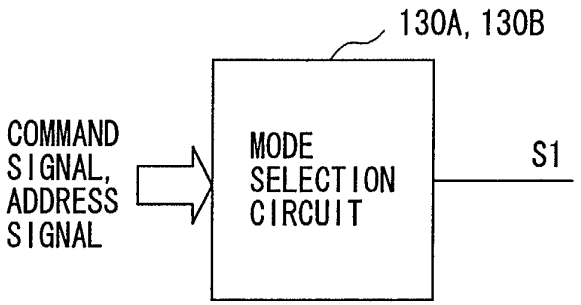

130A, 130B
COMMAND
SIGNAL,
ADDRESS
SIGNAL
MODE
SELECTION
CIRCUIT
S1

FIG.8

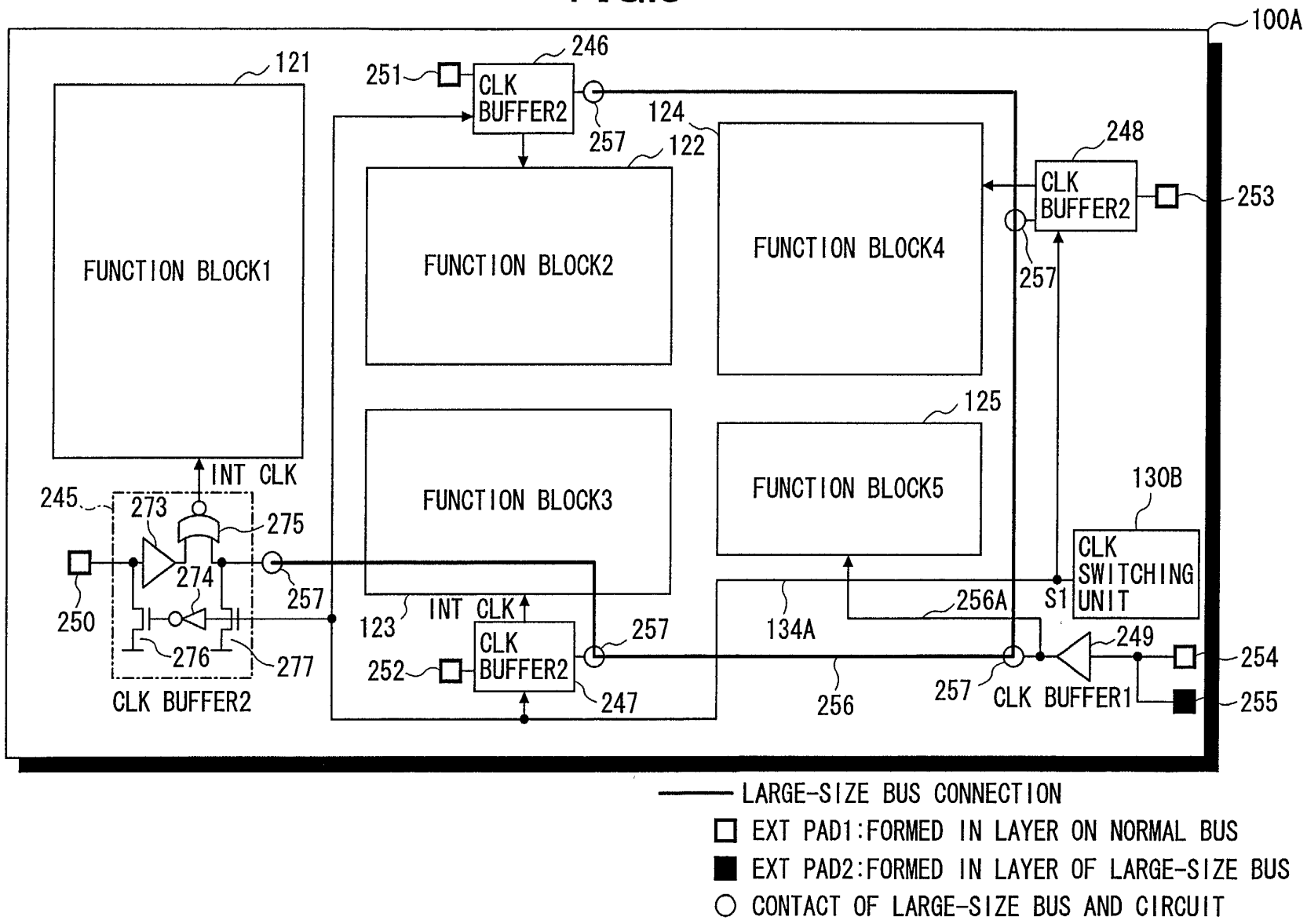

100A
121
FUNCTION BLOCK1
246
251
CLK BUFFER2
257
124
122
FUNCTION BLOCK2
FUNCTION BLOCK4
248
CLK BUFFER2
253
257
125
FUNCTION BLOCK3
FUNCTION BLOCK5
130B
CLK SWITCHING UNIT
INT CLK
245
273
275
274
250
257
276
277
CLK BUFFER2
123
INT CLK
252
CLK BUFFER2
257
247
134A
256A
S1
249
254
255
256
257
CLK BUFFER1
LARGE-SIZE BUS CONNECTION
EXT PAD1:FORMED IN LAYER ON NORMAL BUS
EXT PAD2:FORMED IN LAYER OF LARGE-SIZE BUS
CONTACT OF LARGE-SIZE BUS AND CIRCUIT

FIG.9

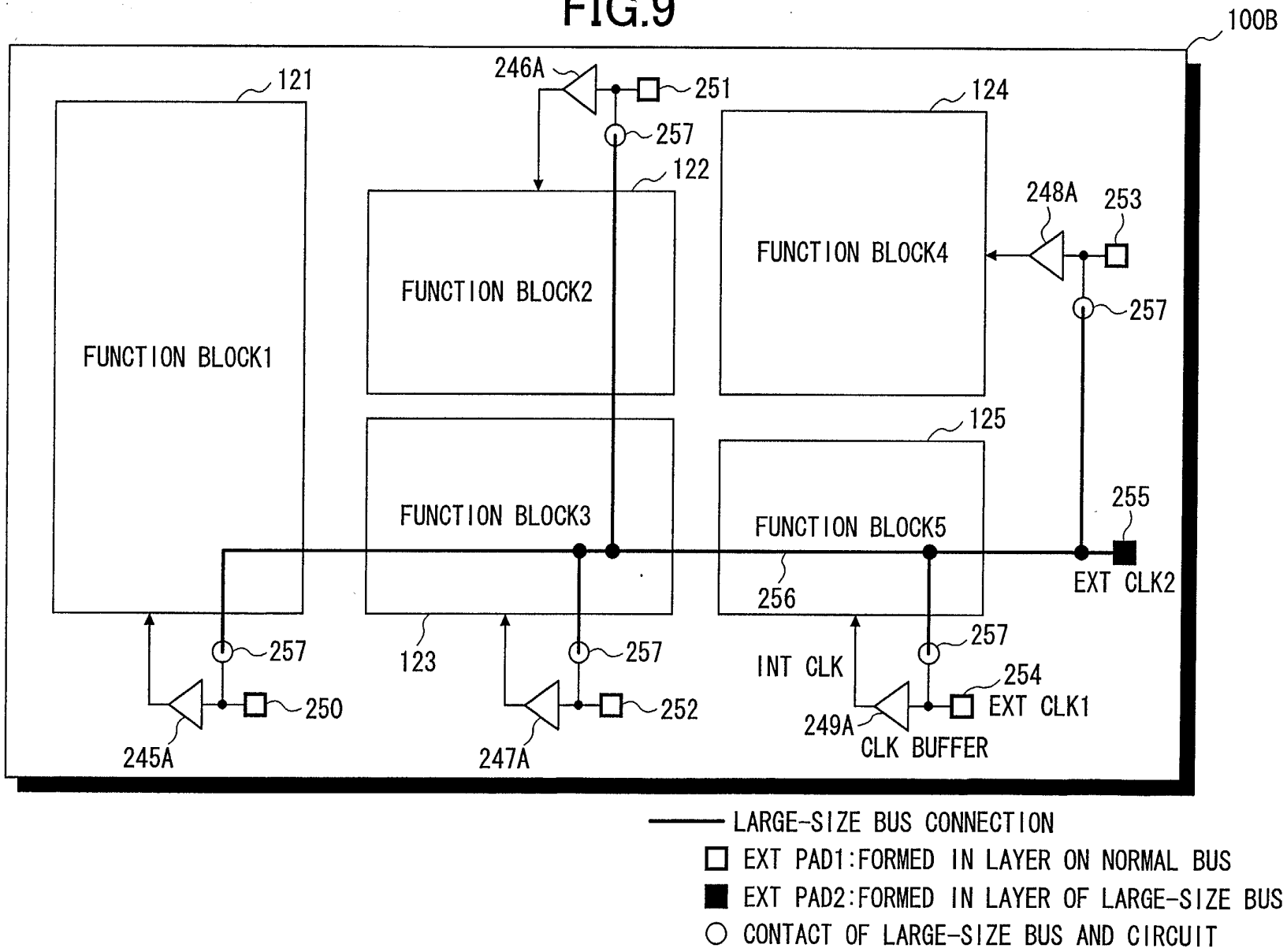

100B
121
246A
251
124
257
122
248A
253
FUNCTION BLOCK4
FUNCTION BLOCK2
FUNCTION BLOCK1
257
125
FUNCTION BLOCK3
FUNCTION BLOCK5
255
256
EXT CLK2
257
123
257
INT CLK
257
254
250
252
EXT CLK1
249A
245A
247A
CLK BUFFER
LARGE-SIZE BUS CONNECTION
EXT PAD1:FORMED IN LAYER ON NORMAL BUS
EXT PAD2:FORMED IN LAYER OF LARGE-SIZE BUS
CONTACT OF LARGE-SIZE BUS AND CIRCUIT

FIG.10

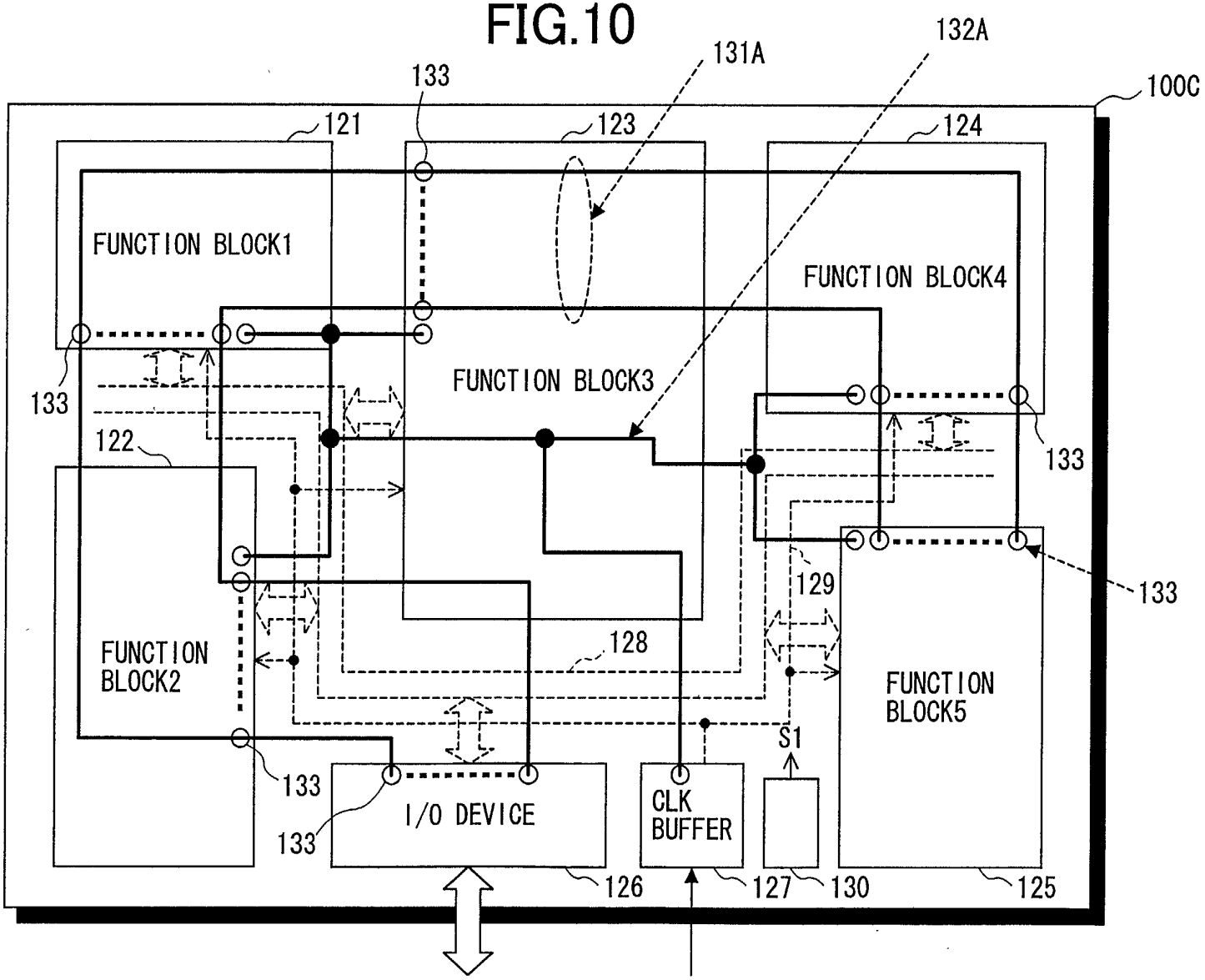

100C
121
123
124
131A
132A
133
FUNCTION BLOCK1
FUNCTION BLOCK3
FUNCTION BLOCK4
FUNCTION BLOCK2
FUNCTION BLOCK5
122
128
129
S1
I/O DEVICE
CLK BUFFER
126
127
130
125

FIG.11

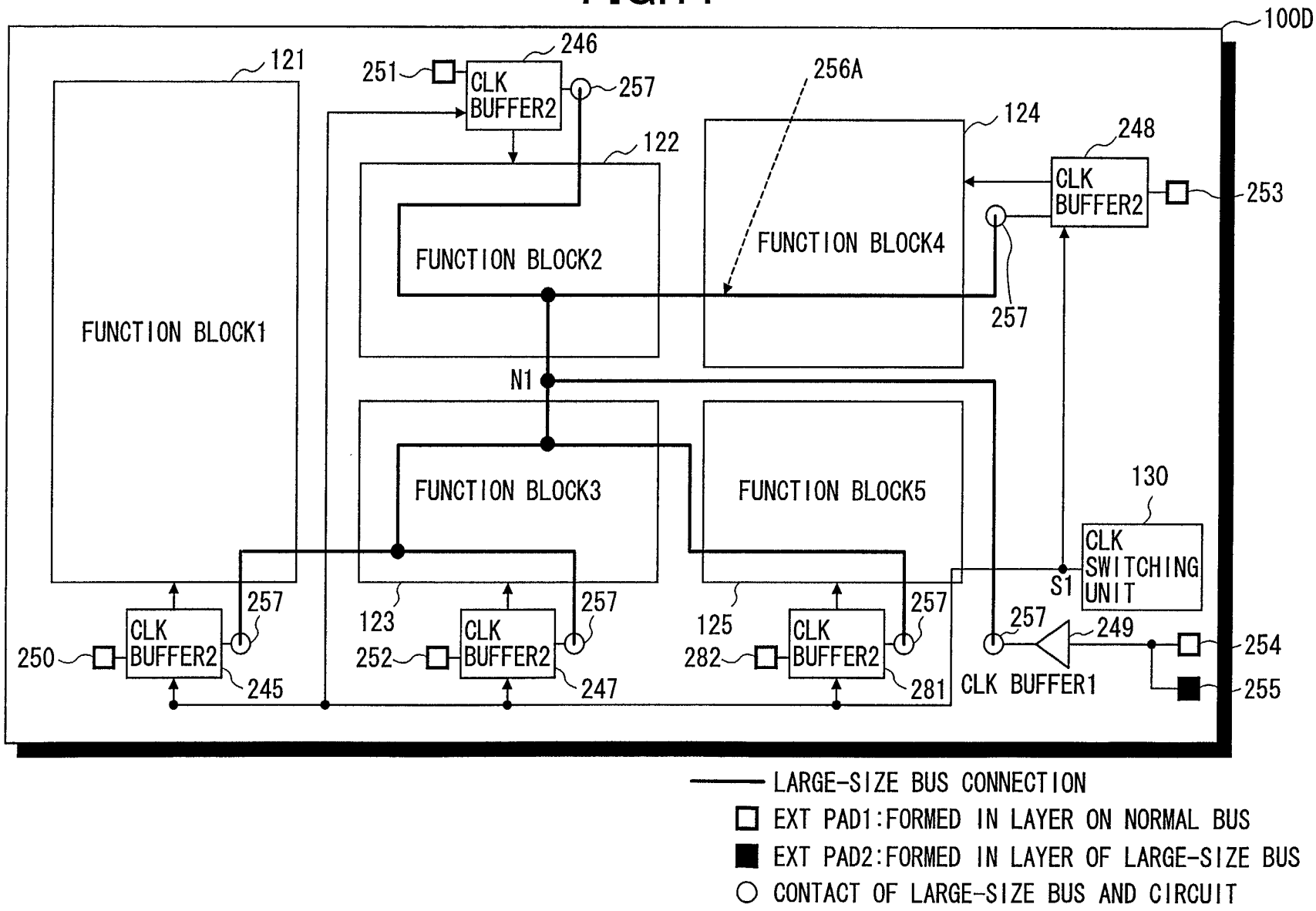

100D
121
246
251
CLK BUFFER2
257
256A
124
248
122
CLK BUFFER2
253
FUNCTION BLOCK2
FUNCTION BLOCK4
FUNCTION BLOCK1
257
N1
FUNCTION BLOCK3
FUNCTION BLOCK5
130
CLK SWITCHING UNIT
S1
123
125
257
257
257
257
CLK BUFFER2
CLK BUFFER2
CLK BUFFER2
250
252
282
245
247
281
CLK BUFFER1
249
254
255
LARGE-SIZE BUS CONNECTION
EXT PAD1:FORMED IN LAYER ON NORMAL BUS
EXT PAD2:FORMED IN LAYER OF LARGE-SIZE BUS
CONTACT OF LARGE-SIZE BUS AND CIRCUIT

FIG.12

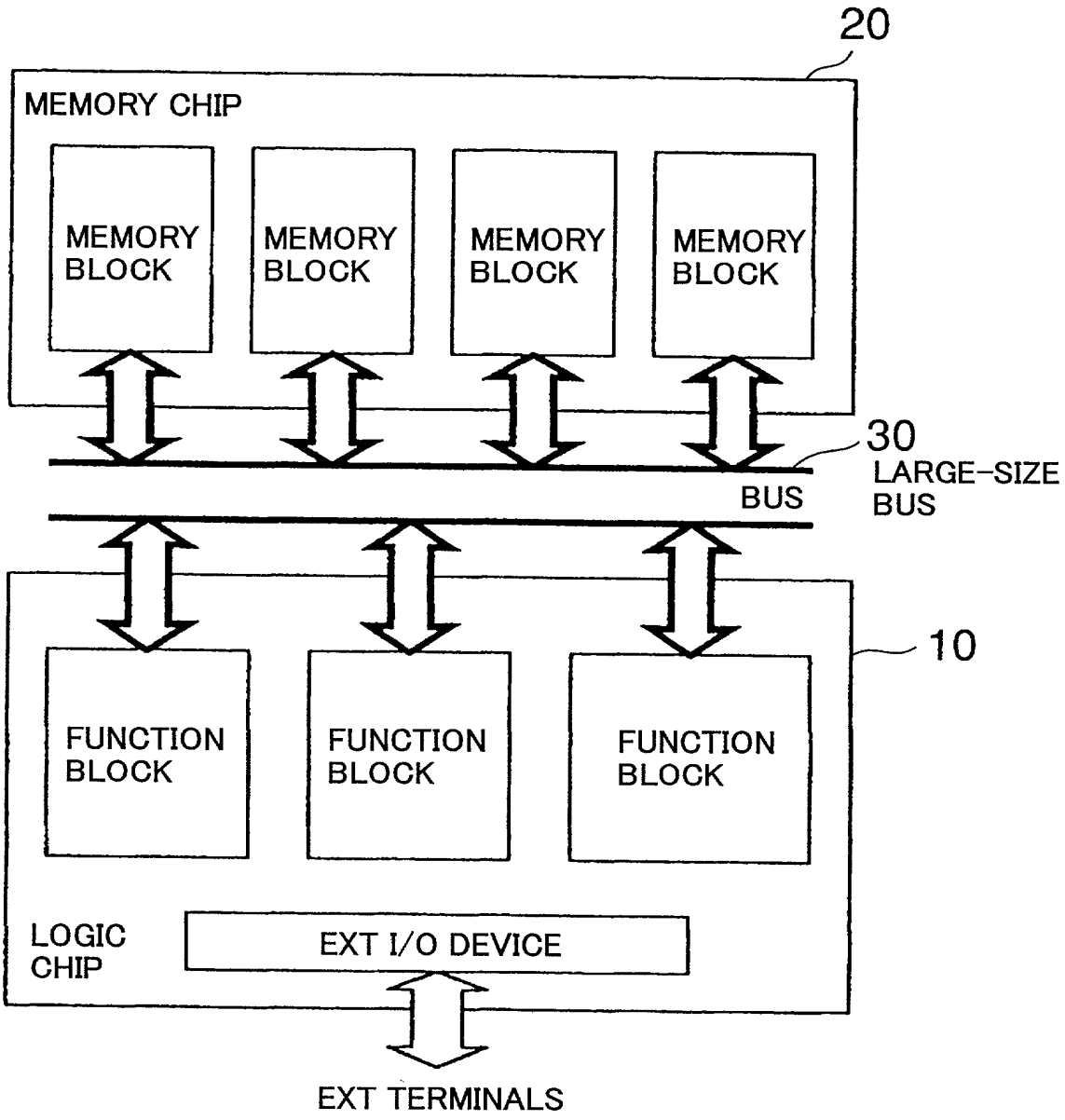

20
MEMORY CHIP
MEMORY BLOCK
MEMORY BLOCK
MEMORY BLOCK
MEMORY BLOCK
30
LARGE-SIZE BUS
BUS
10
FUNCTION BLOCK
FUNCTION BLOCK
FUNCTION BLOCK
LOGIC CHIP
EXT I/O DEVICE
EXT TERMINALS

FIG.13

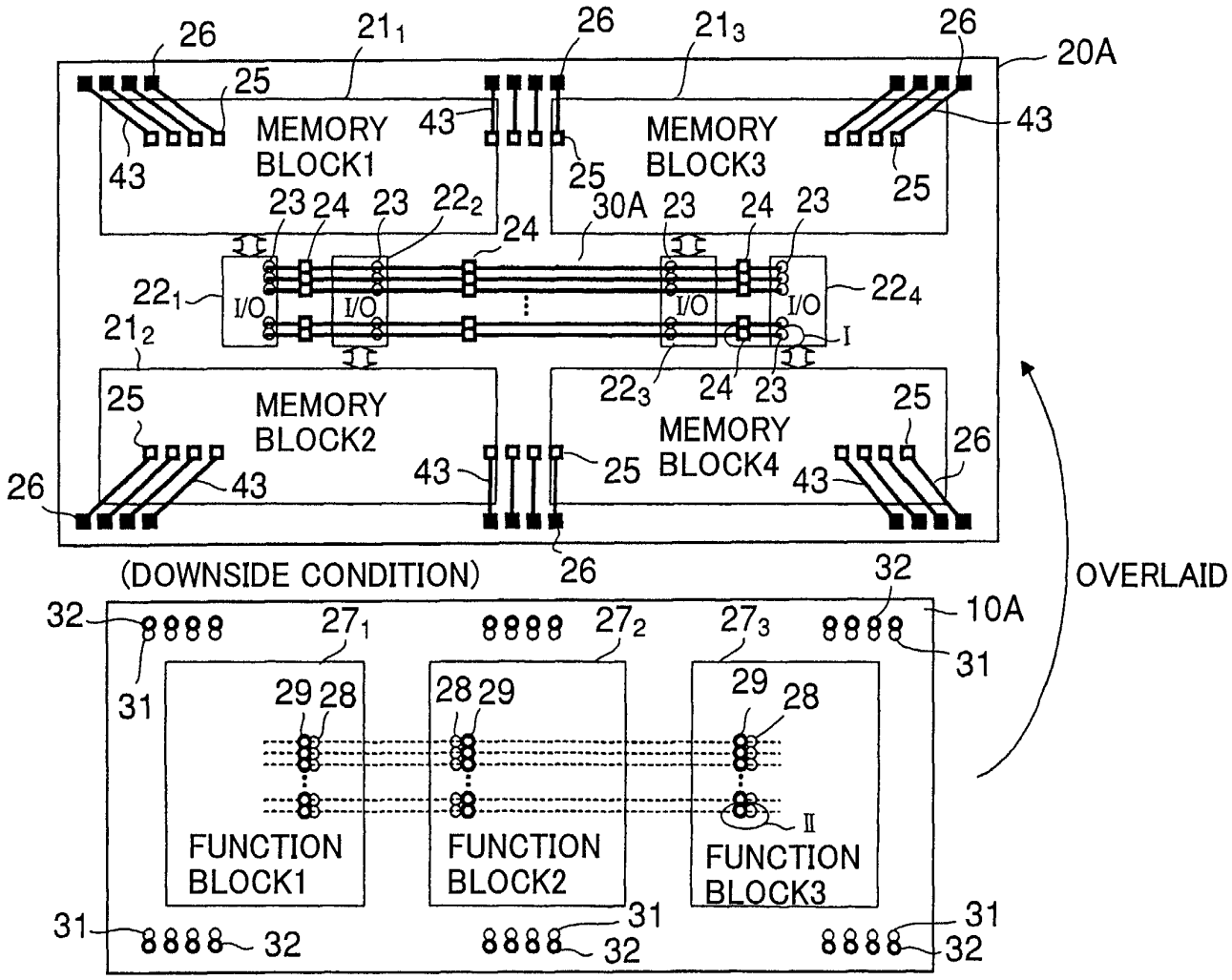

26
21_1
26
21_3
26
20A
25
MEMORY BLOCK1
43
43
MEMORY BLOCK3
43
25
25
23 24 23 22_2
24
30A
23 24 23
22_1
I/O
I/O
I/O
I/O
22_4
21_2
I
22_3 24 23
25
MEMORY BLOCK2
MEMORY BLOCK4
25
26
43
43
26
43
25
43
26
(DOWNSIDE CONDITION)
26
32
OVERLAID
32
8888
27_1
8888
27_2
27_3
8888
10A
31
31
29 28
28 29
29 28
II
FUNCTION BLOCK1
FUNCTION BLOCK2
FUNCTION BLOCK3
31
8888
32
31
8888
32
31
8888
32

FIG. 14

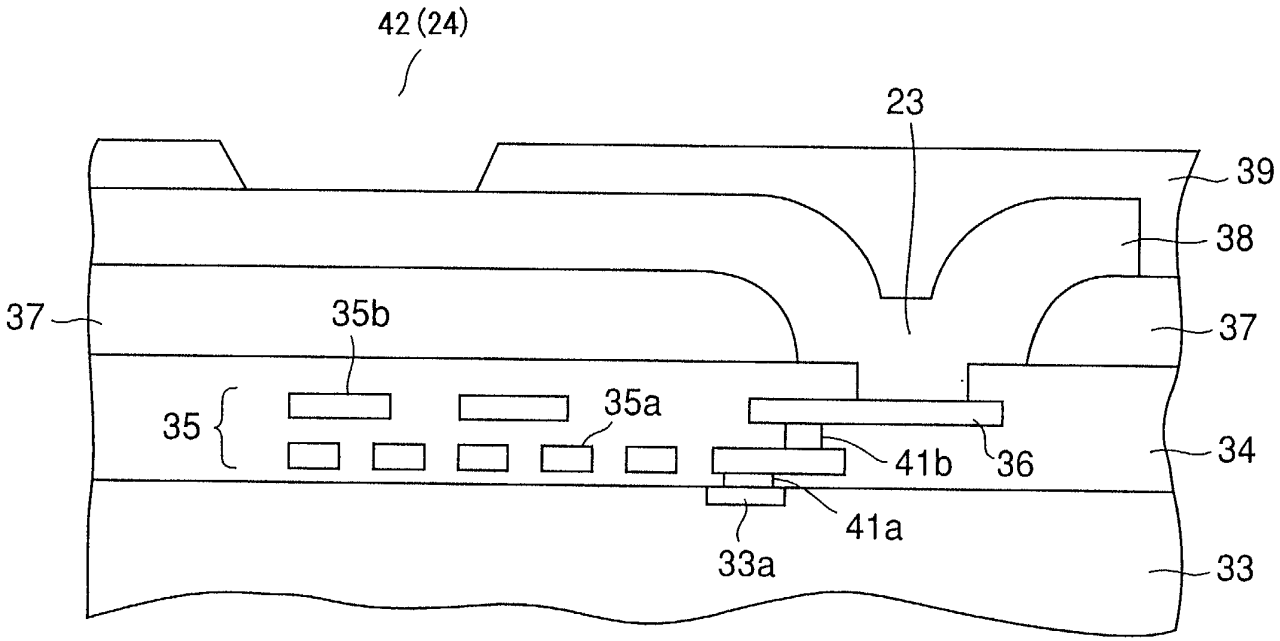


FIG. 15

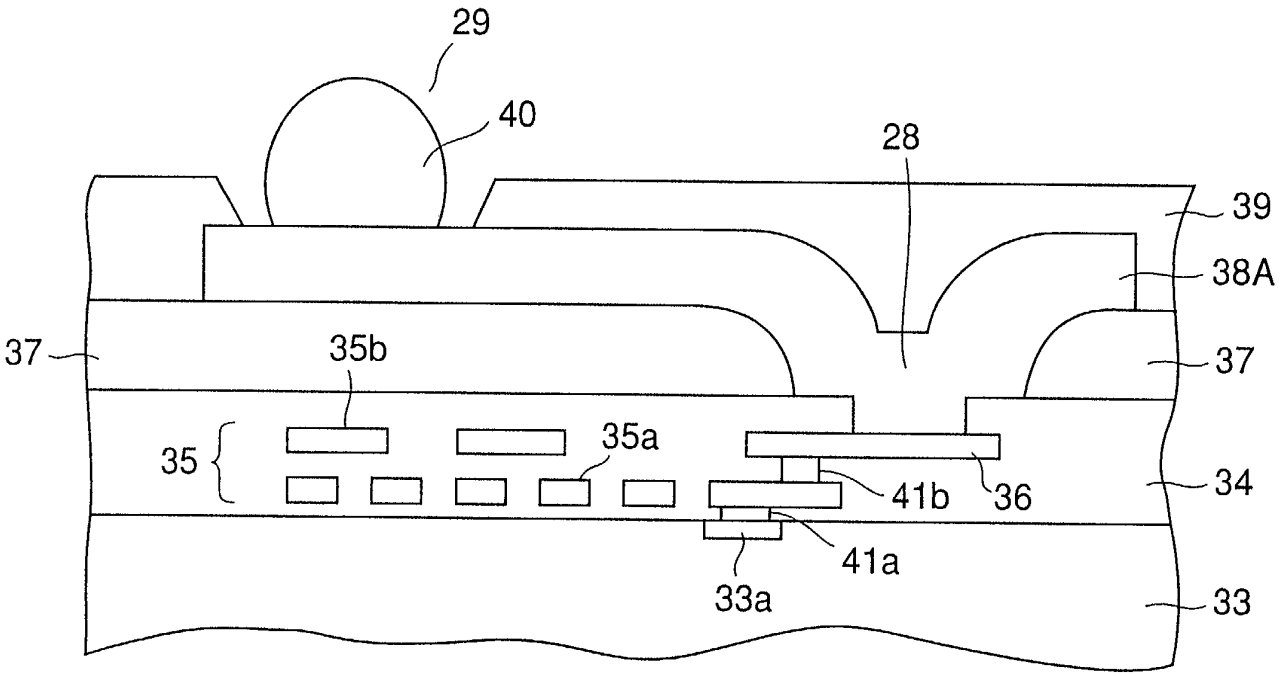


FIG.16

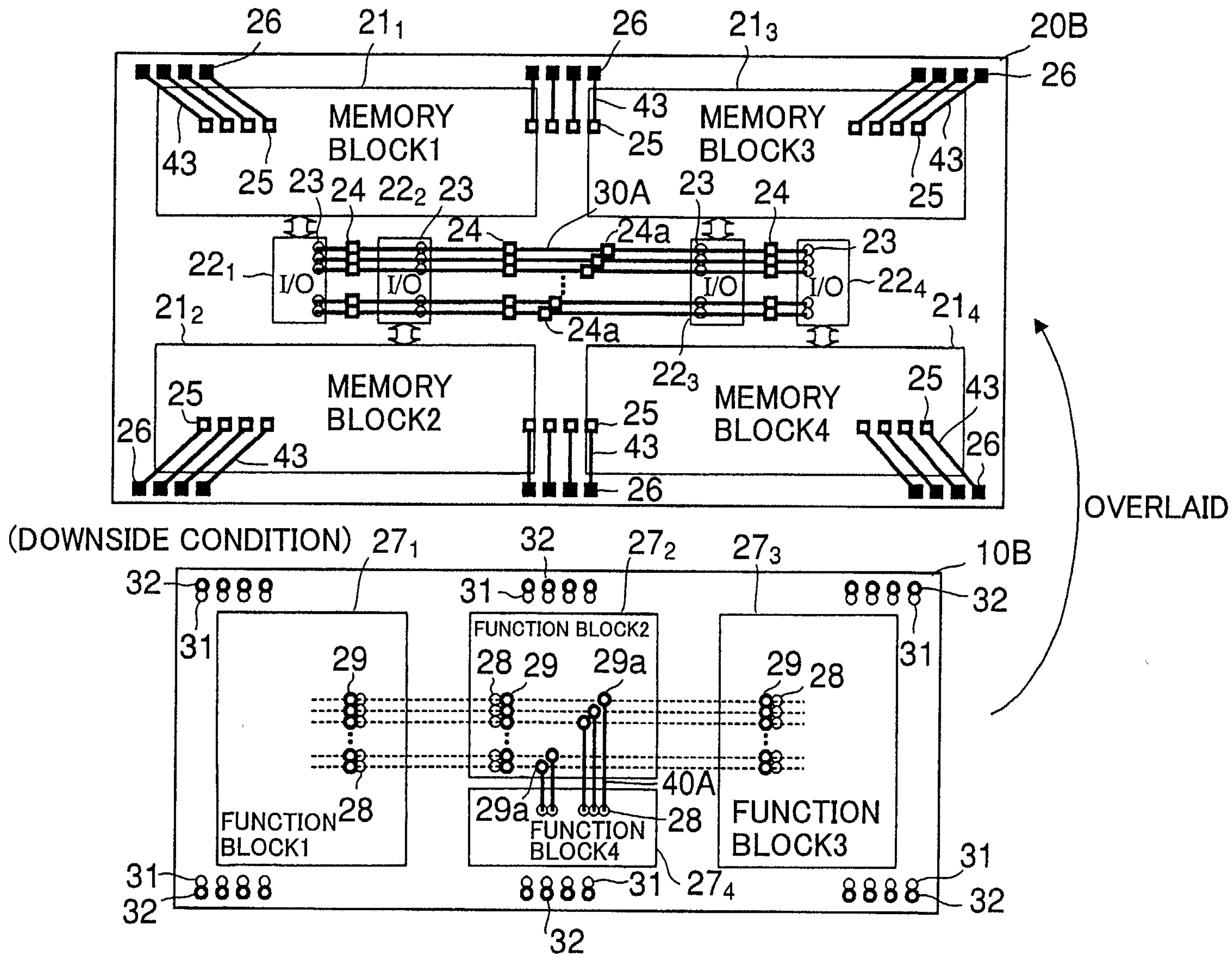

20B
26
21₁
21₂
21₃
21₄
MEMORY BLOCK1
MEMORY BLOCK2
MEMORY BLOCK3
MEMORY BLOCK4
43
25
23
24
22₁
22₂
22₃
22₄
I/O
30A
24a
OVERLAID
(DOWNSIDE CONDITION)
10B
27₁
27₂
27₃
27₄
32
31
FUNCTION BLOCK1
FUNCTION BLOCK2
FUNCTION BLOCK3
FUNCTION BLOCK4
29
28
29a
40A

FIG.17

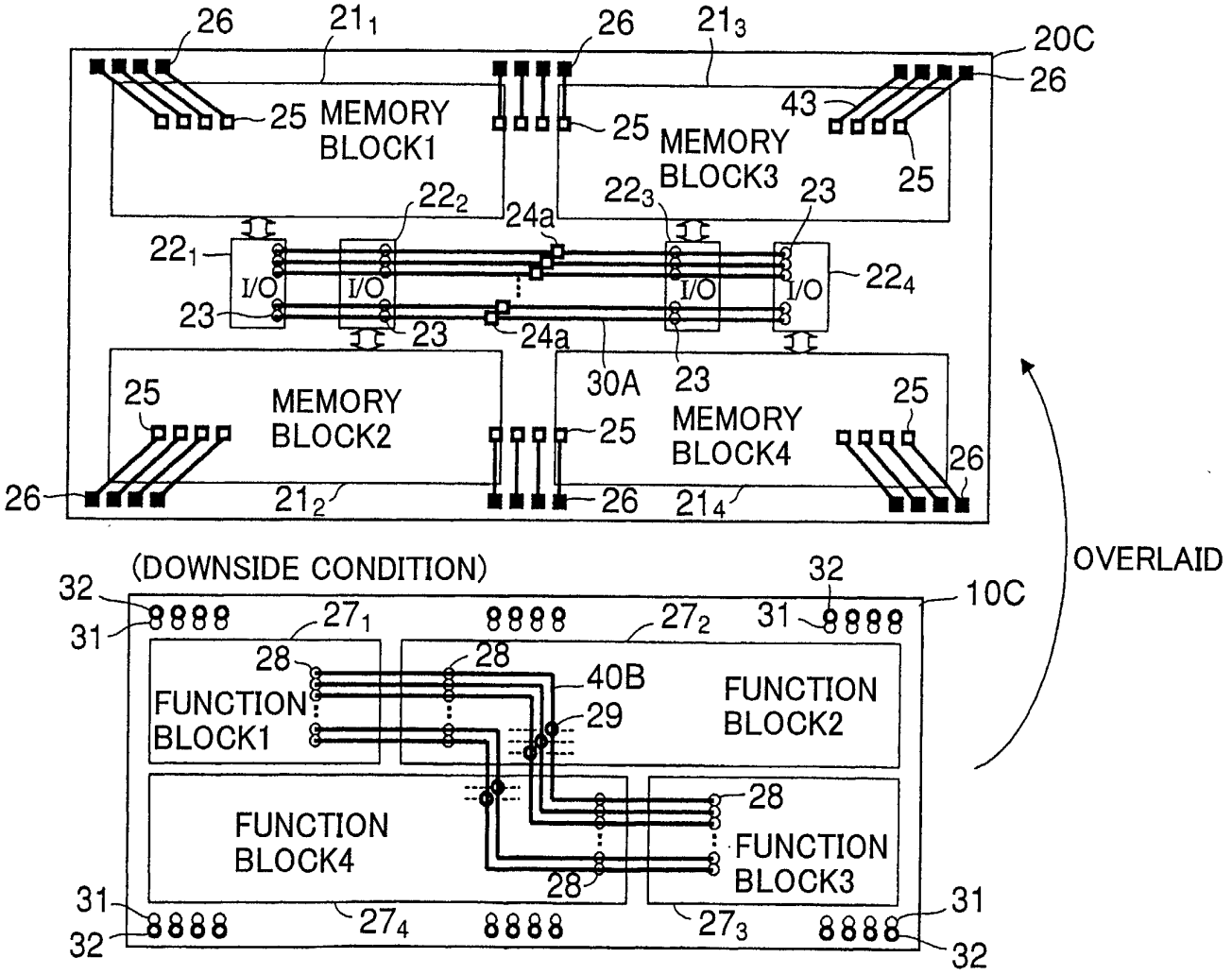

26
21_1
26
21_3
20C
26
25 MEMORY BLOCK1
25
MEMORY BLOCK3
43
25
22_2
24a
22_3
23
22_1
I/O
I/O
I/O
I/O
22_4
23
23
24a
30A
23
25
MEMORY BLOCK2
25
MEMORY BLOCK4
25
26
26
21_2
26
21_4
OVERLAID
(DOWNSIDE CONDITION)
32
32
10C
31
8888
27_1
8888
27_2
31
8888
28
28
40B
FUNCTION BLOCK1
29
FUNCTION BLOCK2
28
FUNCTION BLOCK4
FUNCTION BLOCK3
28
31
31
8888
27_4
8888
27_3
8888
32
32

FIG.18

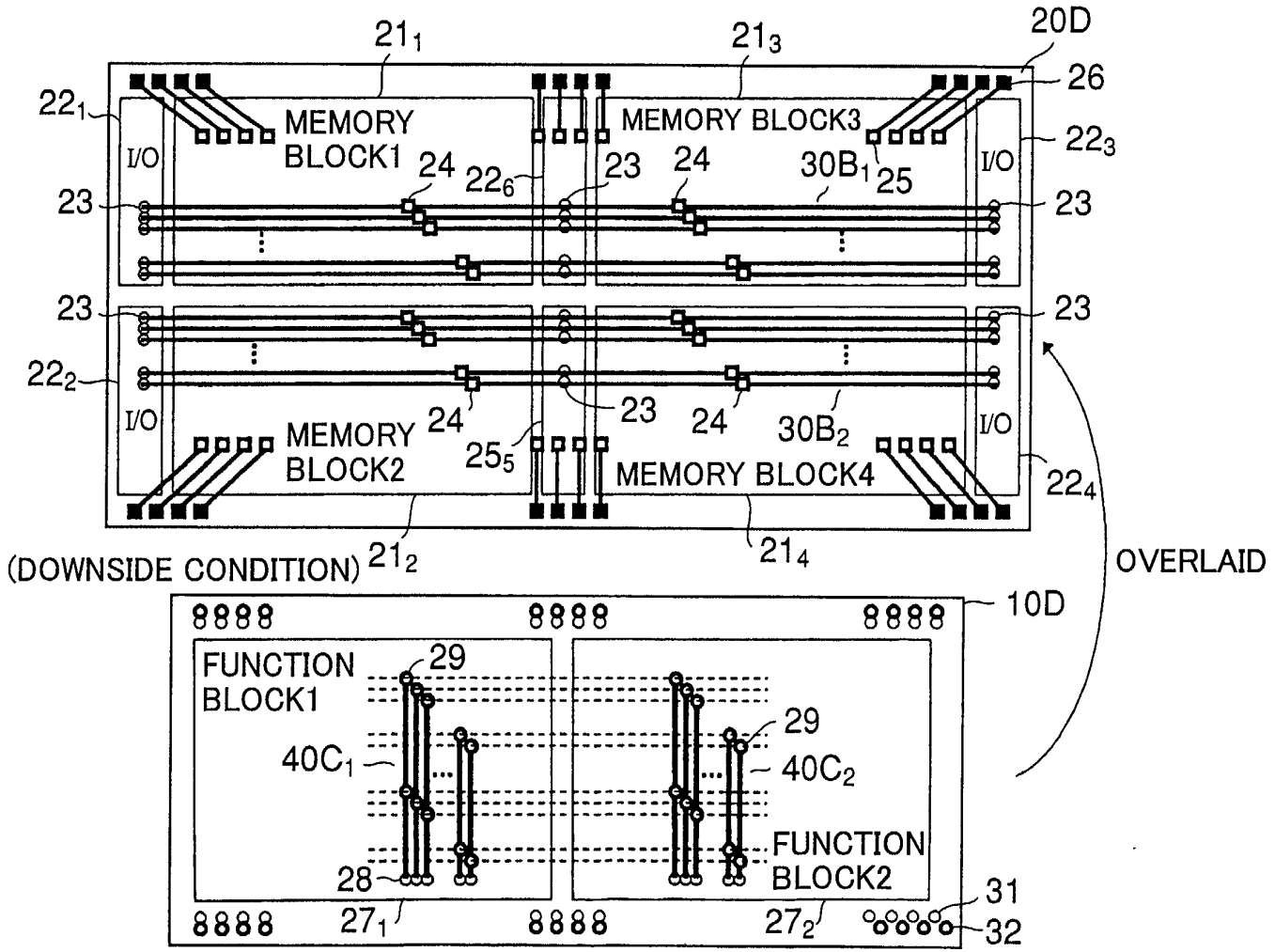

21_1
21_3
20D
26
22_1
MEMORY BLOCK1
MEMORY BLOCK3
I/O
24
22_6
23
24
$30B_1$
25
I/O
22_3
23
23
23
22_2
I/O
24
23
24
$30B_2$
I/O
MEMORY BLOCK2
25_5
MEMORY BLOCK4
22_4
(DOWNSIDE CONDITION)
21_2
21_4
OVERLAID
10D
8888
8888
8888
FUNCTION BLOCK1
29
$40C_1$
28
29
$40C_2$
FUNCTION BLOCK2
31
32
8888
27_1
8888
27_2

FIG.19

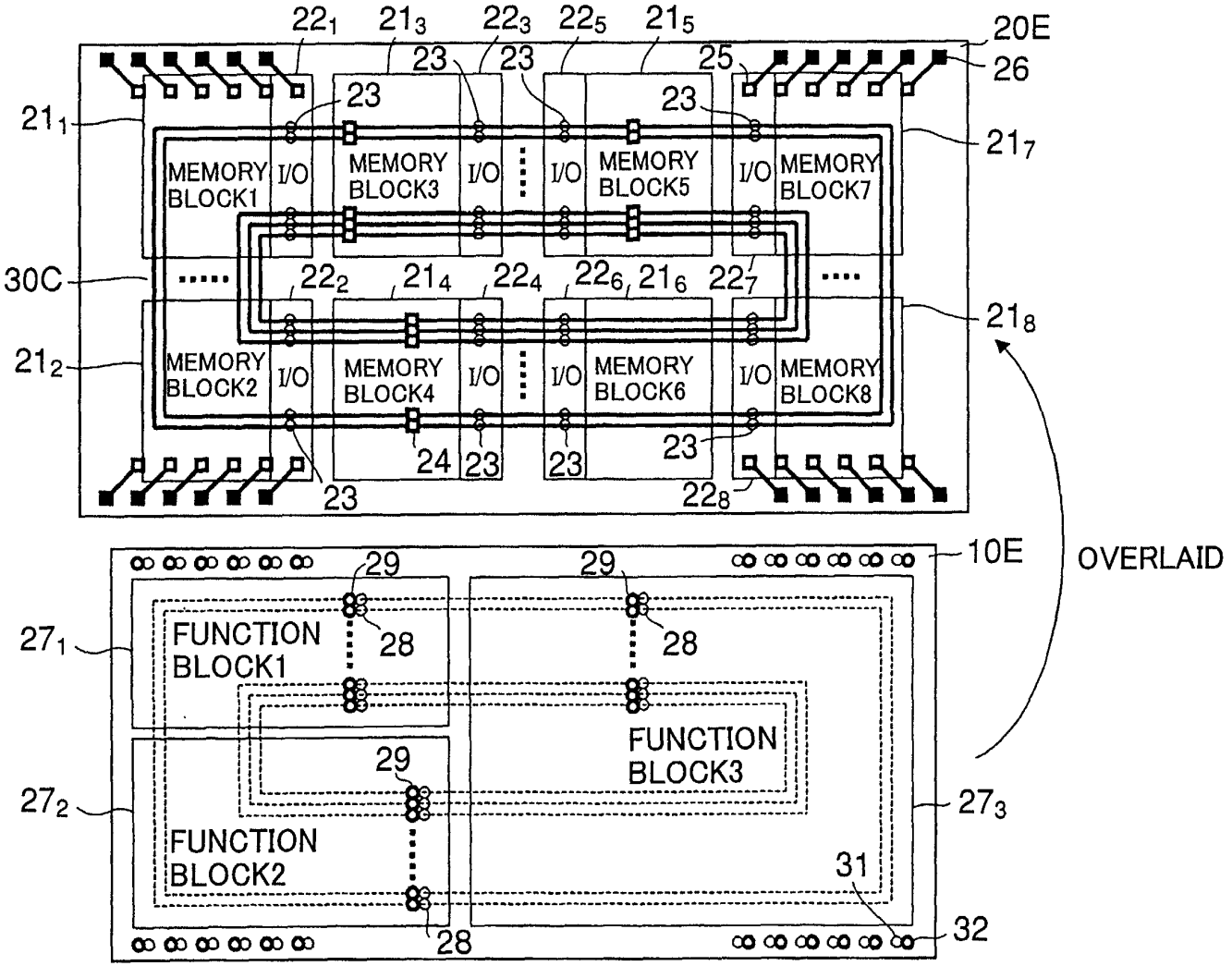

22_1 21_3 22_3 22_5 21_5
20E
26
25
23
21_1
21_7
MEMORY BLOCK1
I/O
MEMORY BLOCK3
I/O
I/O
MEMORY BLOCK5
I/O
MEMORY BLOCK7
30C
22_2 21_4 22_4 22_6 21_6 22_7
21_8
21_2
MEMORY BLOCK2
MEMORY BLOCK4
MEMORY BLOCK6
MEMORY BLOCK8
24
22_8
10E
OVERLAID
29
28
27_1
FUNCTION BLOCK1
FUNCTION BLOCK3
27_2
FUNCTION BLOCK2
27_3
31
32

FIG.20

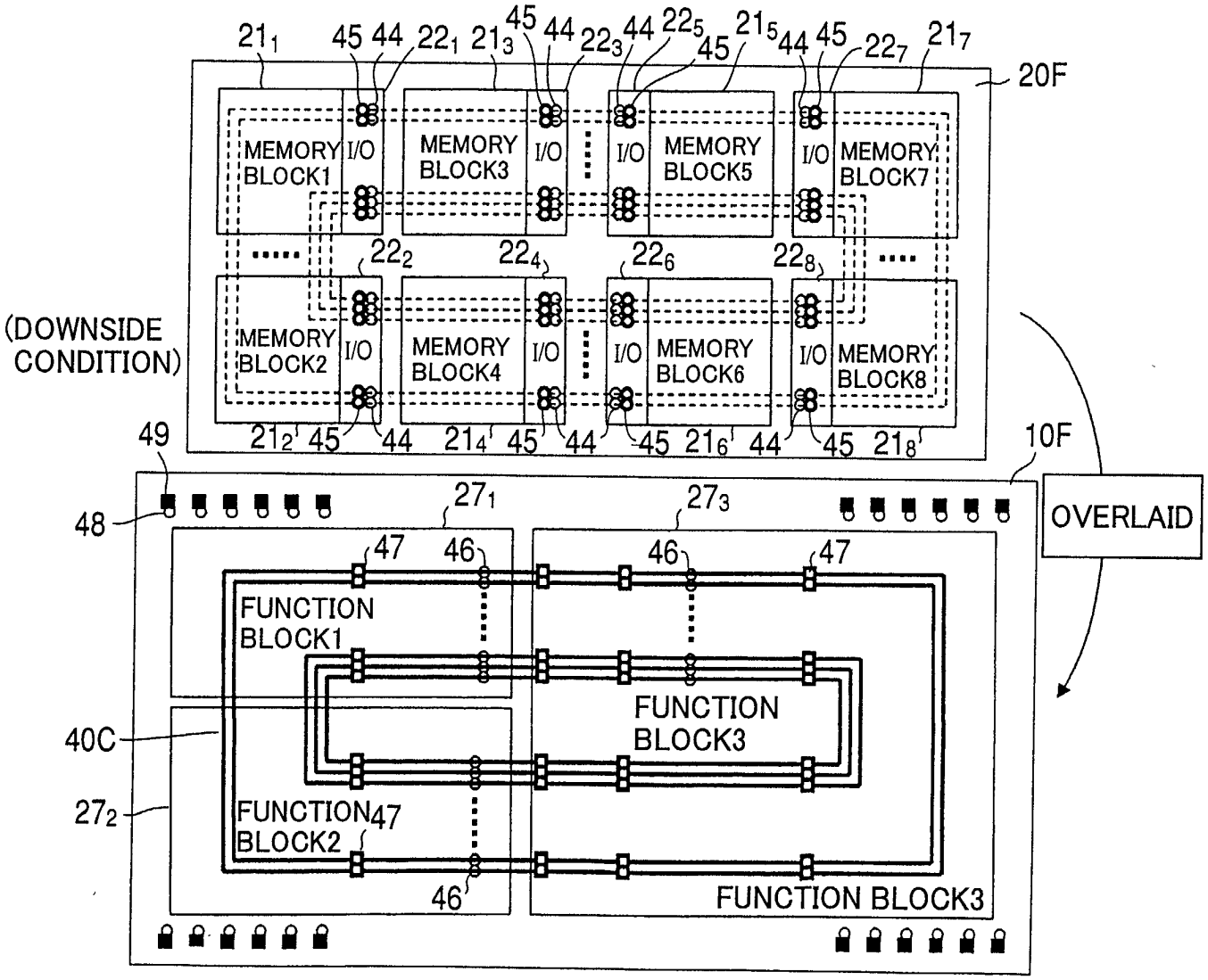

21_1
45
44
22_1
21_3
45
44
22_3
44
22_5
45
21_5
44
45
22_7
21_7
20F
MEMORY BLOCK1
I/O
MEMORY BLOCK3
I/O
I/O
MEMORY BLOCK5
I/O
MEMORY BLOCK7
22_2
22_4
22_6
22_8
(DOWNSIDE CONDITION)
MEMORY BLOCK2
I/O
MEMORY BLOCK4
I/O
I/O
MEMORY BLOCK6
I/O
MEMORY BLOCK8
49
21_2
45
44
21_4
45
44
45
21_6
44
45
21_8
10F
OVERLAID
48
27_1
27_3
47
46
46
47
FUNCTION BLOCK1
FUNCTION BLOCK3
40C
27_2
FUNCTION BLOCK2
47
46
FUNCTION BLOCK3

FIG.21

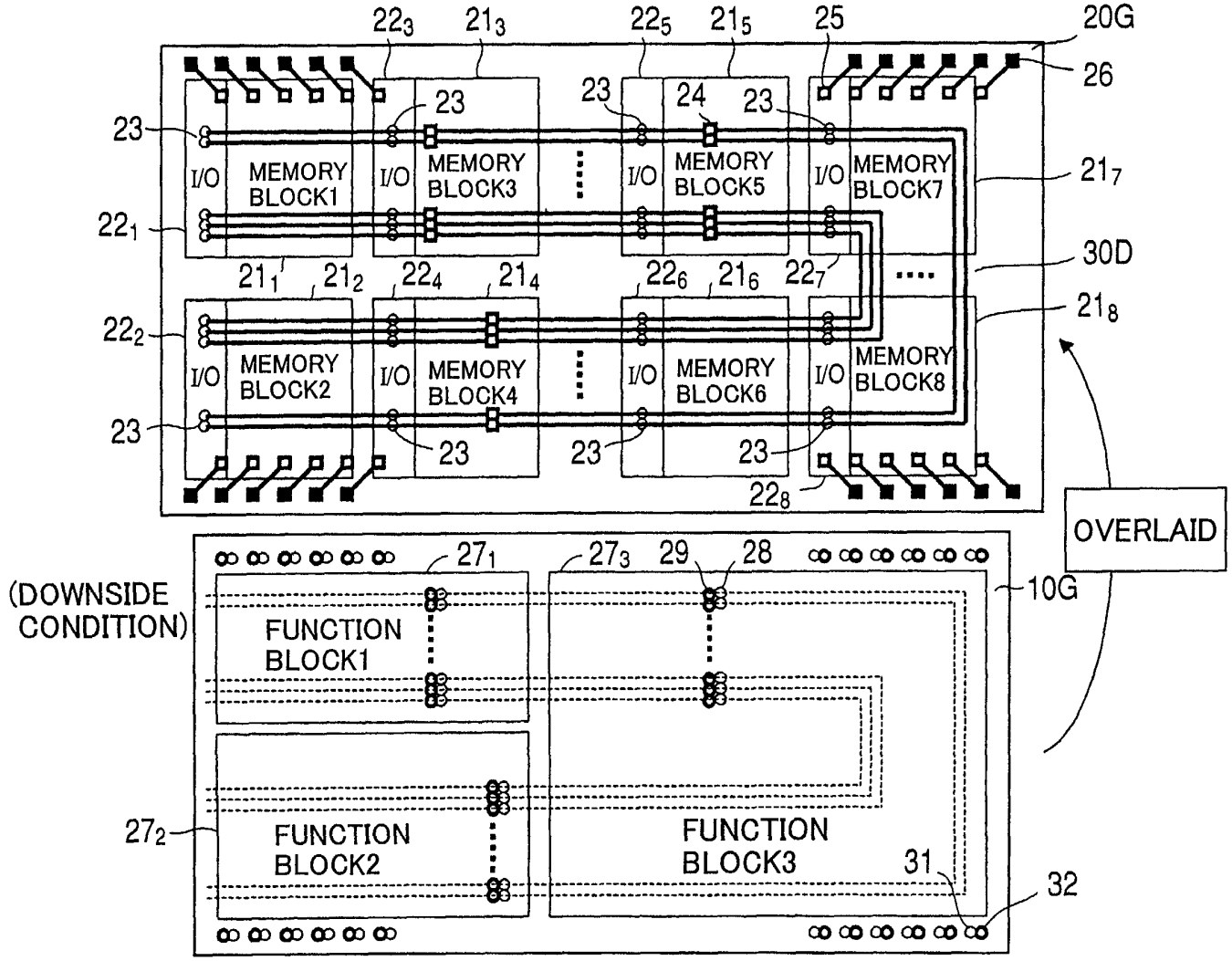

20G
26
25
22_3
21_3
22_5
21_5
23
24
21_7
30D
21_8
22_1
22_2
21_1
21_2
22_4
21_4
22_6
21_6
22_7
22_8
I/O
MEMORY BLOCK1
MEMORY BLOCK2
MEMORY BLOCK3
MEMORY BLOCK4
MEMORY BLOCK5
MEMORY BLOCK6
MEMORY BLOCK7
MEMORY BLOCK8
OVERLAID
(DOWNSIDE CONDITION)
27_1
27_3
29
28
10G
FUNCTION BLOCK1
FUNCTION BLOCK2
FUNCTION BLOCK3
27_2
31
32

FIG.22

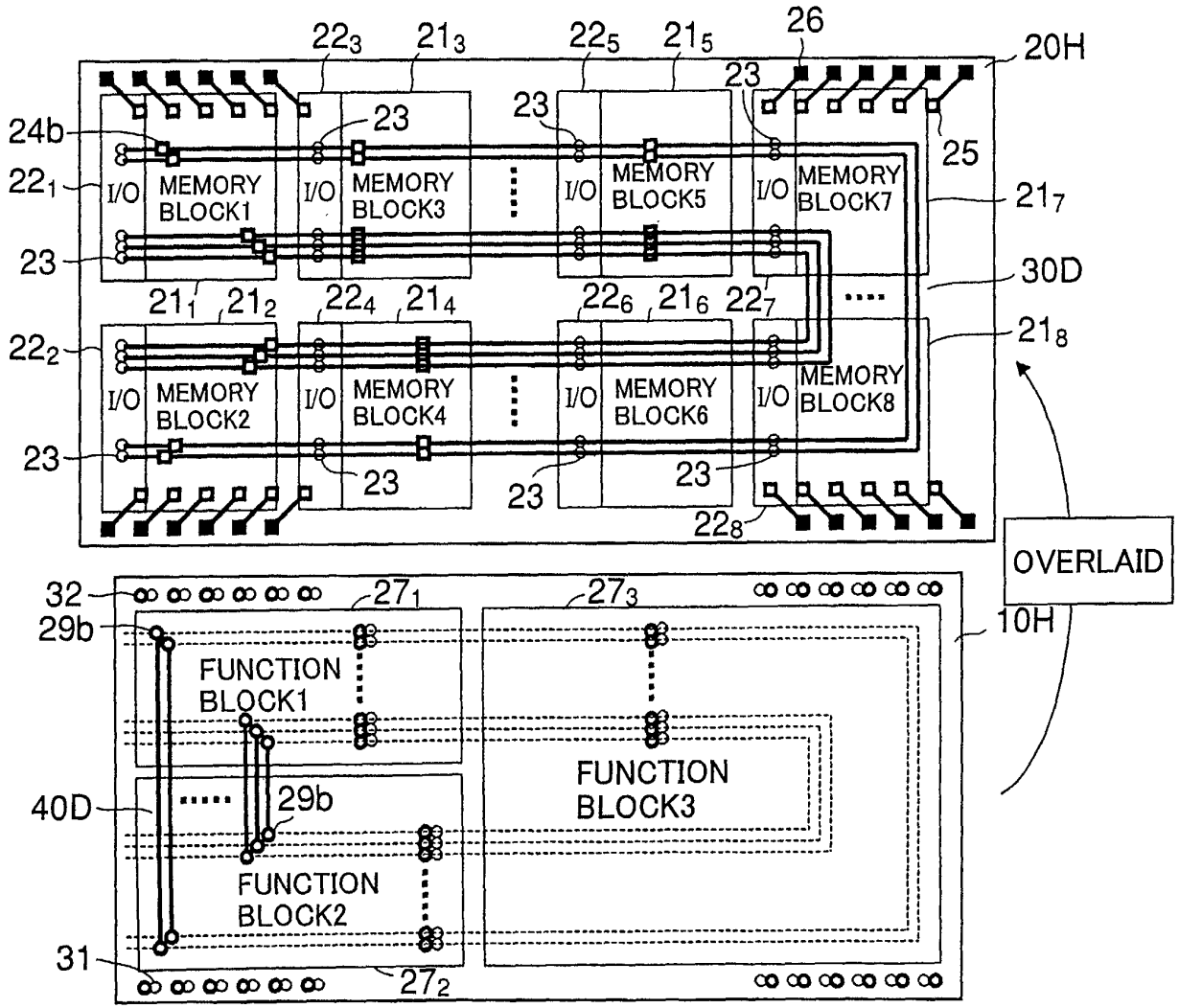

20H
24b
23
25
26
I/O
MEMORY BLOCK1
MEMORY BLOCK2
MEMORY BLOCK3
MEMORY BLOCK4
MEMORY BLOCK5
MEMORY BLOCK6
MEMORY BLOCK7
MEMORY BLOCK8
30D
OVERLAID
10H
32
29b
FUNCTION BLOCK1
FUNCTION BLOCK2
FUNCTION BLOCK3
40D
31

FIG.23

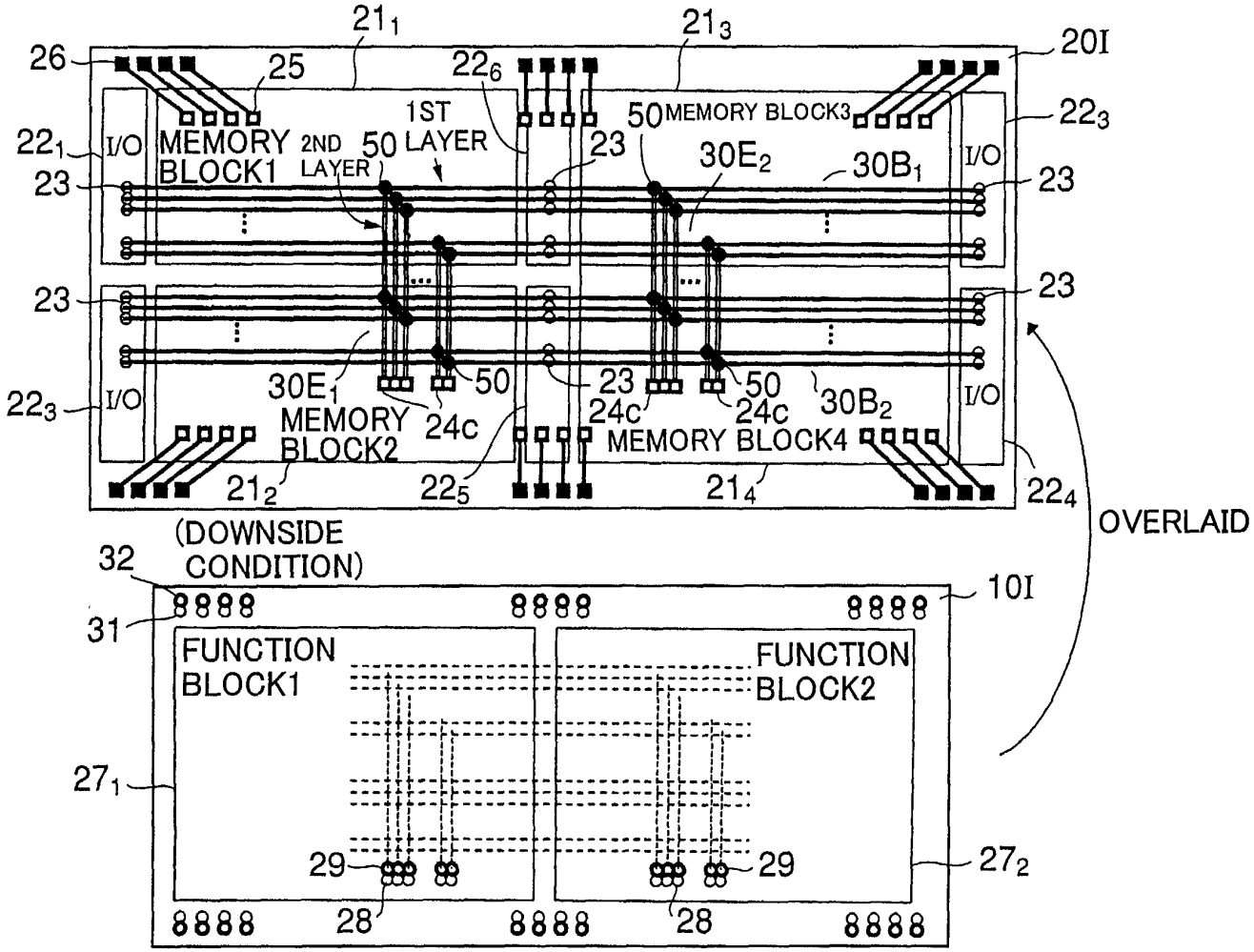

21_1
21_3
26
25
22_6
20I
50
MEMORY BLOCK3
22_3
22_1
I/O
MEMORY BLOCK1
2ND LAYER
50
1ST LAYER
23
$30E_2$
$30B_1$
I/O
23
23
23
$30E_1$
50
23
50
$30B_2$
I/O
22_3
I/O
MEMORY BLOCK2
24c
24c
24c
MEMORY BLOCK4
21_2
22_5
21_4
22_4
OVERLAID
(DOWNSIDE CONDITION)
32
10I
31
FUNCTION BLOCK1
FUNCTION BLOCK2
27_1
29
29
27_2
28
28

FIG. 24

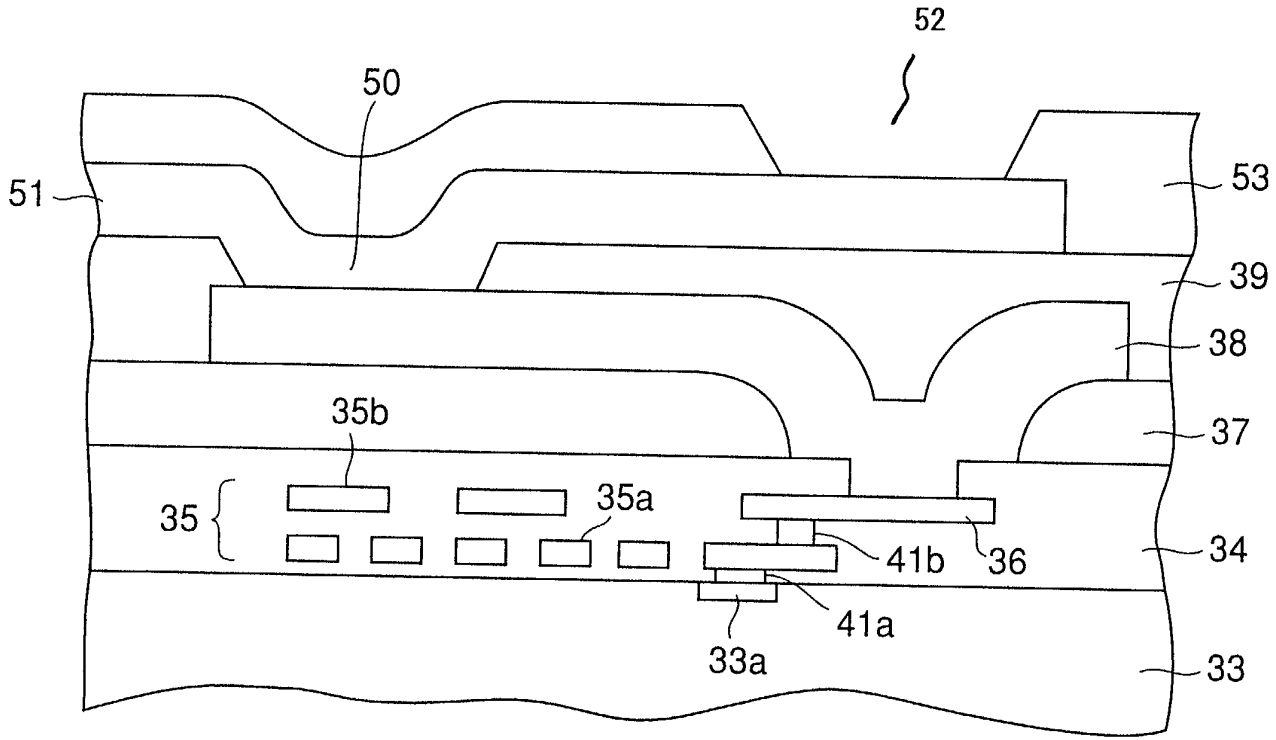


FIG.25

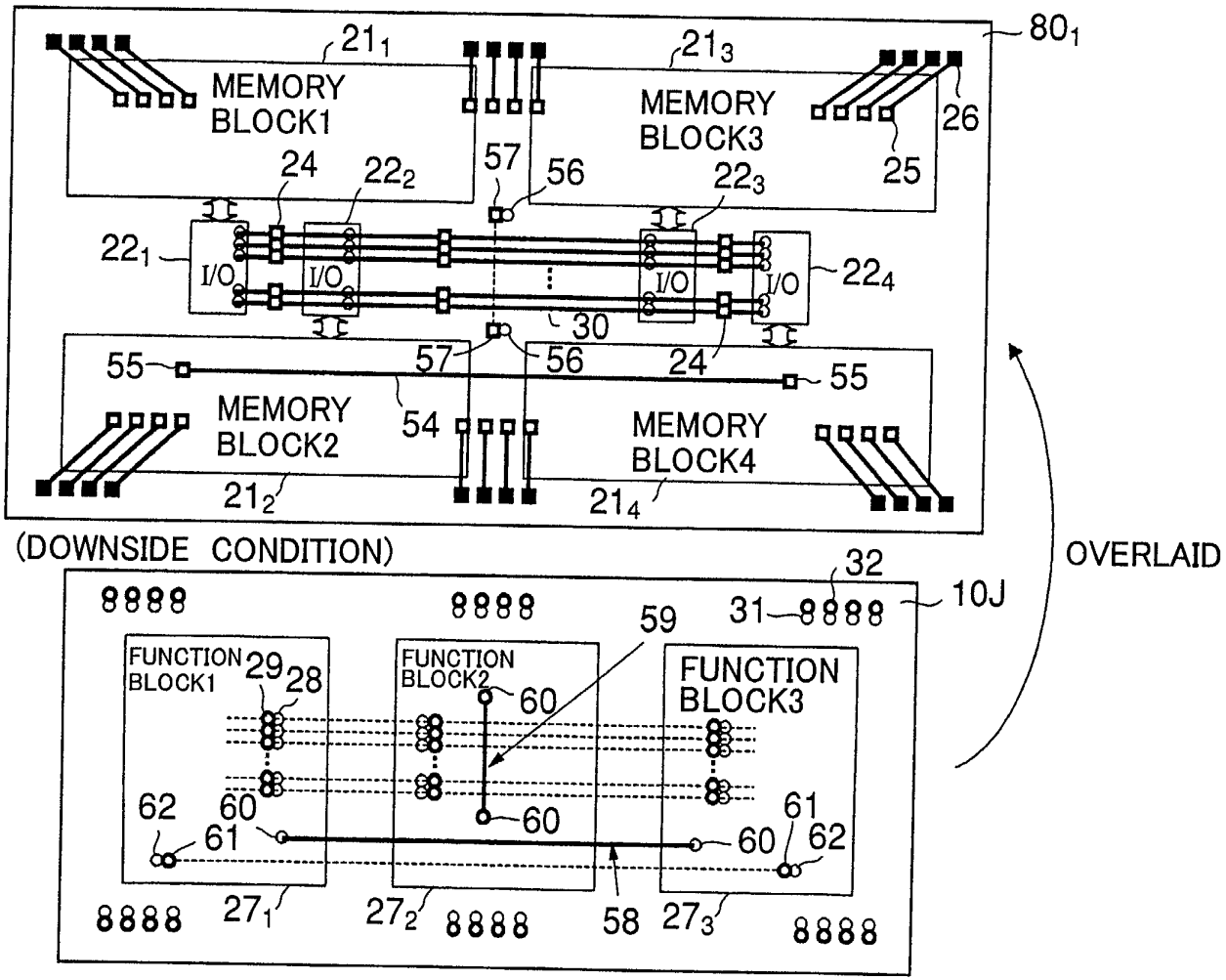

MEMORY BLOCK1
MEMORY BLOCK3
MEMORY BLOCK2
MEMORY BLOCK4
I/O
(DOWNSIDE CONDITION)
OVERLAID
FUNCTION BLOCK1
FUNCTION BLOCK2
FUNCTION BLOCK3
8888

FIG.26

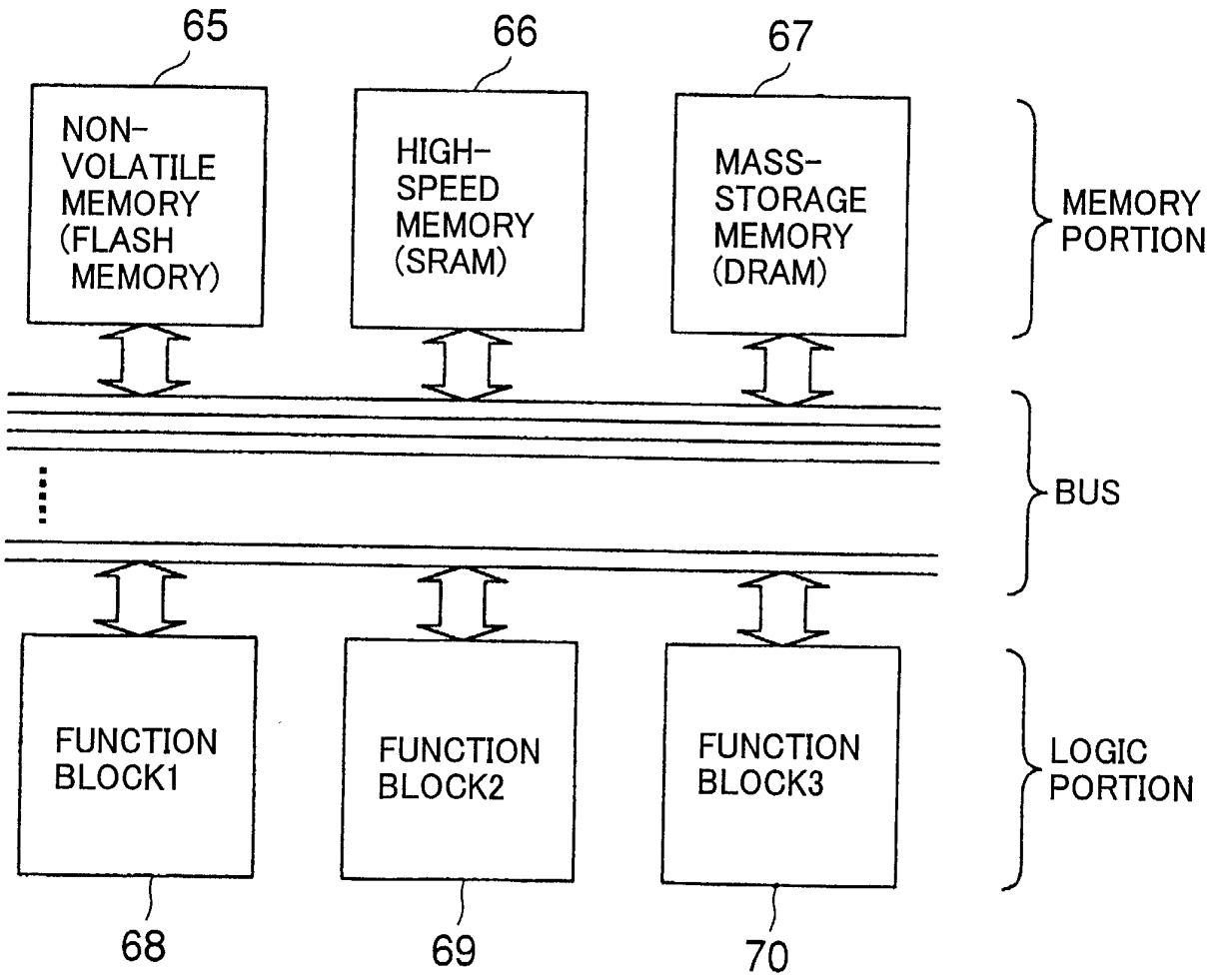

65
66
67
NON-VOLATILE MEMORY (FLASH MEMORY)
HIGH-SPEED MEMORY (SRAM)
MASS-STORAGE MEMORY (DRAM)
MEMORY PORTION
BUS
FUNCTION BLOCK1
FUNCTION BLOCK2
FUNCTION BLOCK3
LOGIC PORTION
68
69
70

FIG.27

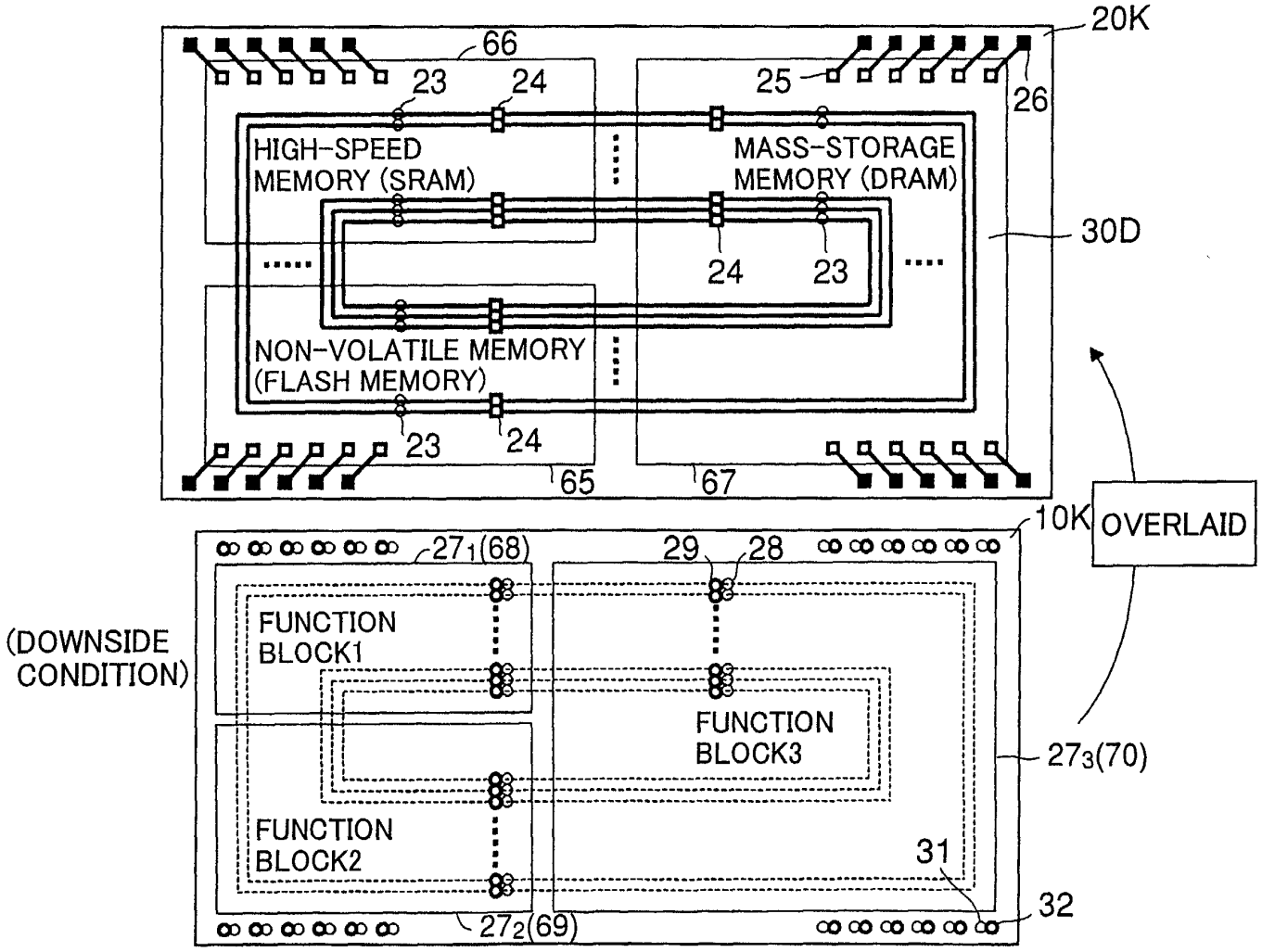

20K
66
23
24
25
26
HIGH-SPEED
MEMORY (SRAM)
MASS-STORAGE
MEMORY (DRAM)
30D
24
23
NON-VOLATILE MEMORY
(FLASH MEMORY)
23
24
65
67
10K
OVERLAID
(DOWNSIDE
CONDITION)
27₁(68)
29
28
FUNCTION
BLOCK1
FUNCTION
BLOCK3
27₃(70)
FUNCTION
BLOCK2
31
32
27₂(69)

FIG.28

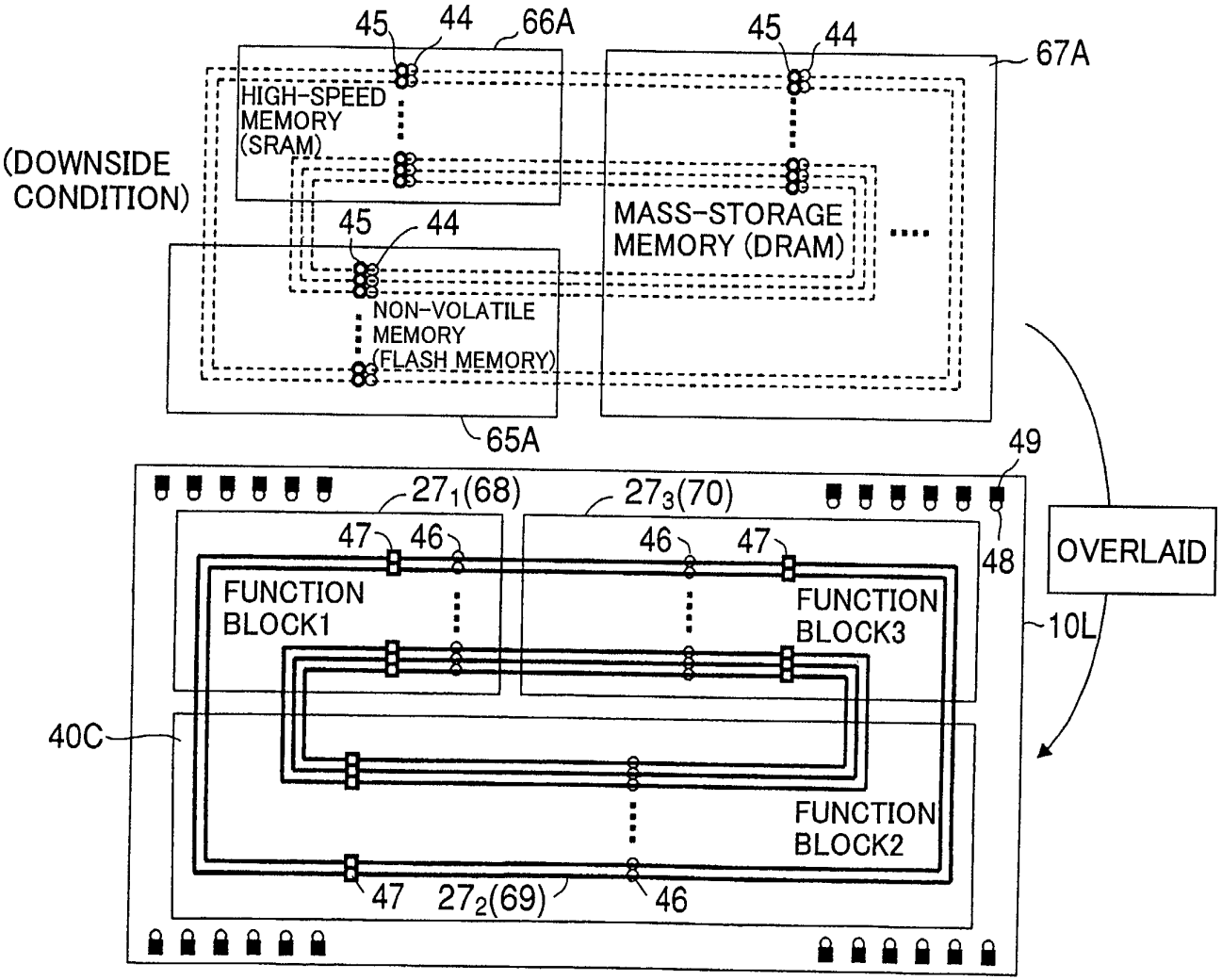

45
44
66A
45
44
67A
HIGH-SPEED MEMORY (SRAM)
(DOWNSIDE CONDITION)
MASS-STORAGE MEMORY (DRAM)
....
45
44
NON-VOLATILE MEMORY (FLASH MEMORY)
65A
49
27_1(68)
27_3(70)
47
46
46
47
48
OVERLAID
FUNCTION BLOCK1
FUNCTION BLOCK3
10L
40C
FUNCTION BLOCK2
47
27_2(69)
46

FIG.29

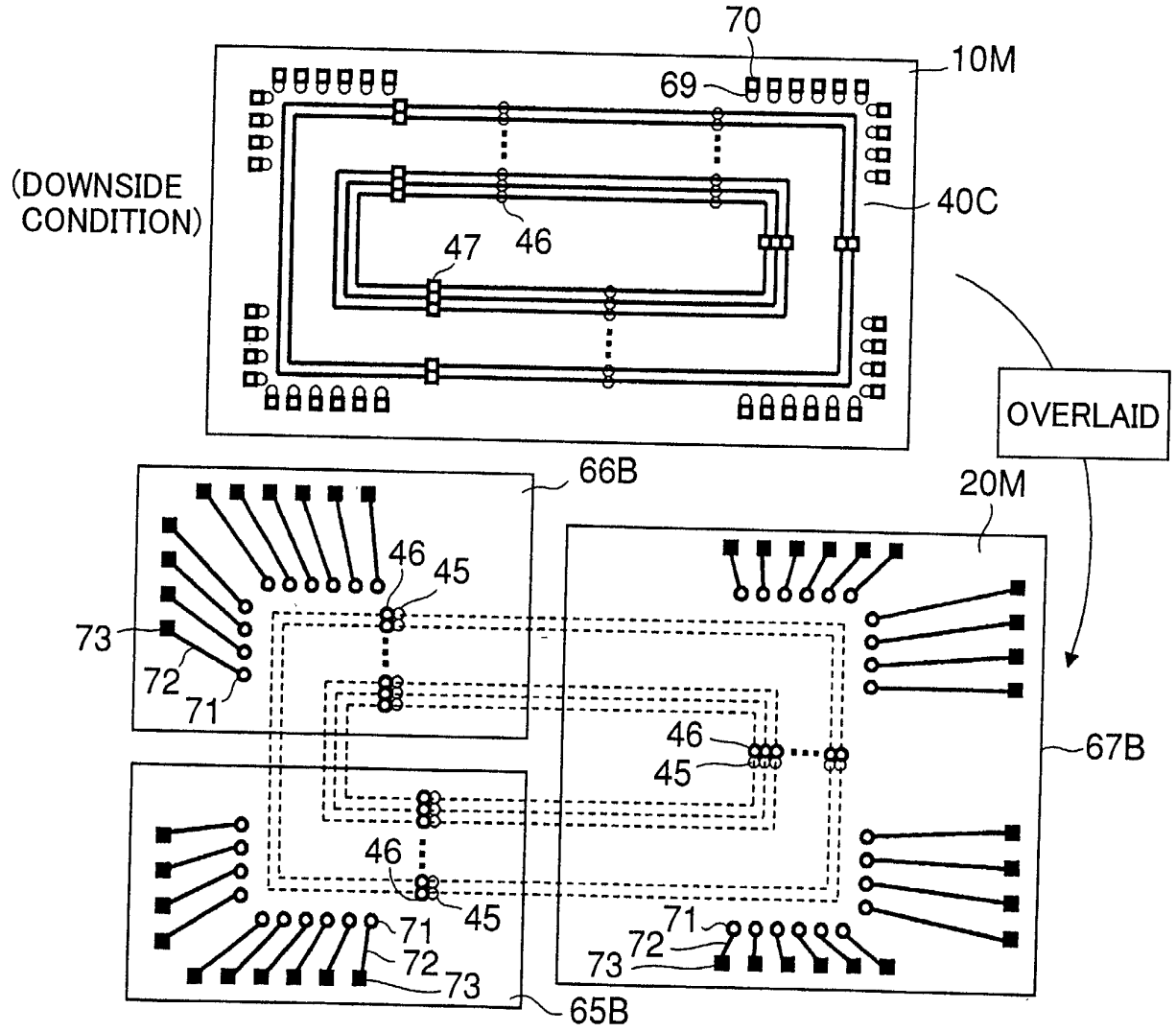

70
10M
69
(DOWNSIDE CONDITION)
40C
47
46
OVERLAID
66B
20M
46
45
73
72
71
67B
46
45
46
45
71
72
73
71
72
73
65B

FIG. 30

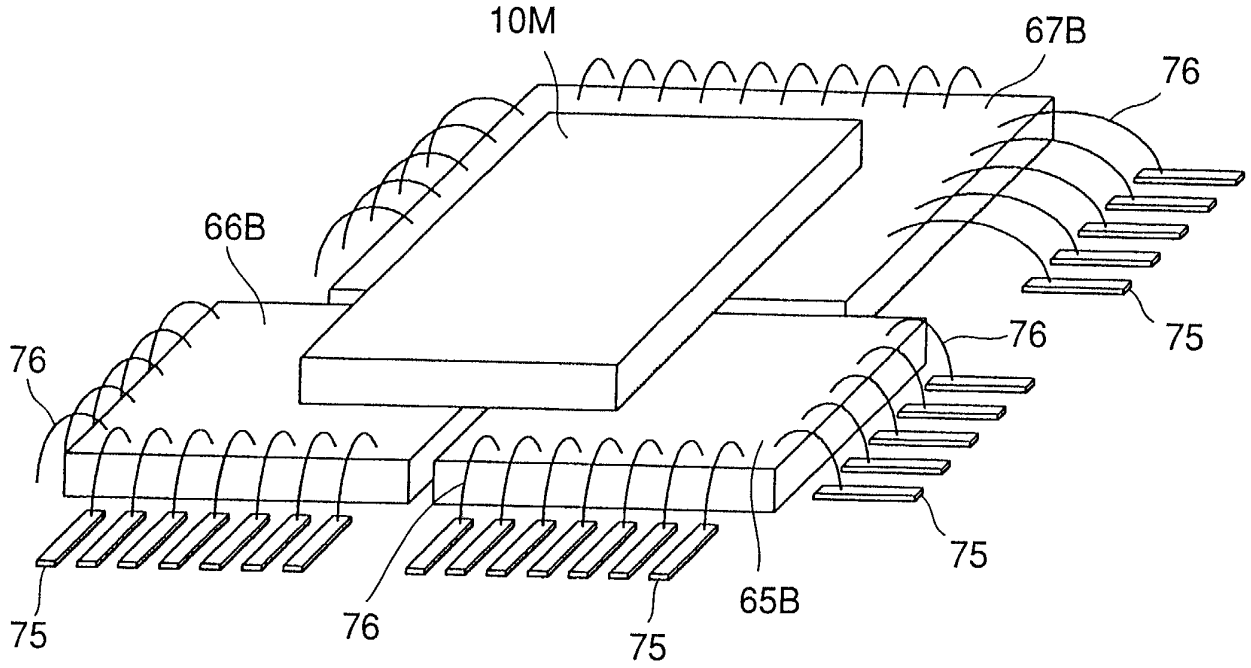


FIG. 31

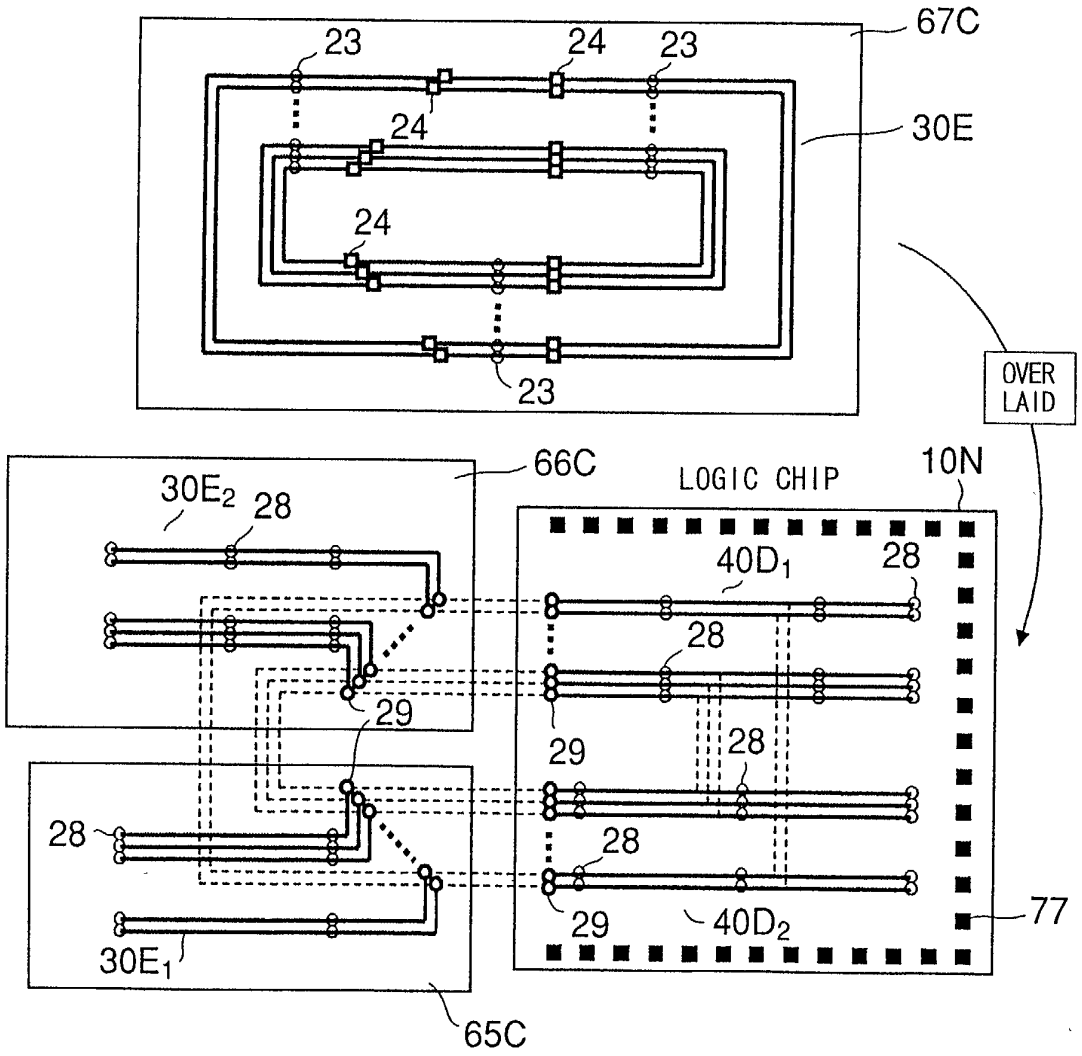

67C
23
24
23
24
30E
24
23
OVER LAID
66C
LOGIC CHIP
10N
30E2
28
40D1
28
28
29
29
28
28
28
28
29
40D2
77
30E1
65C

FIG. 32

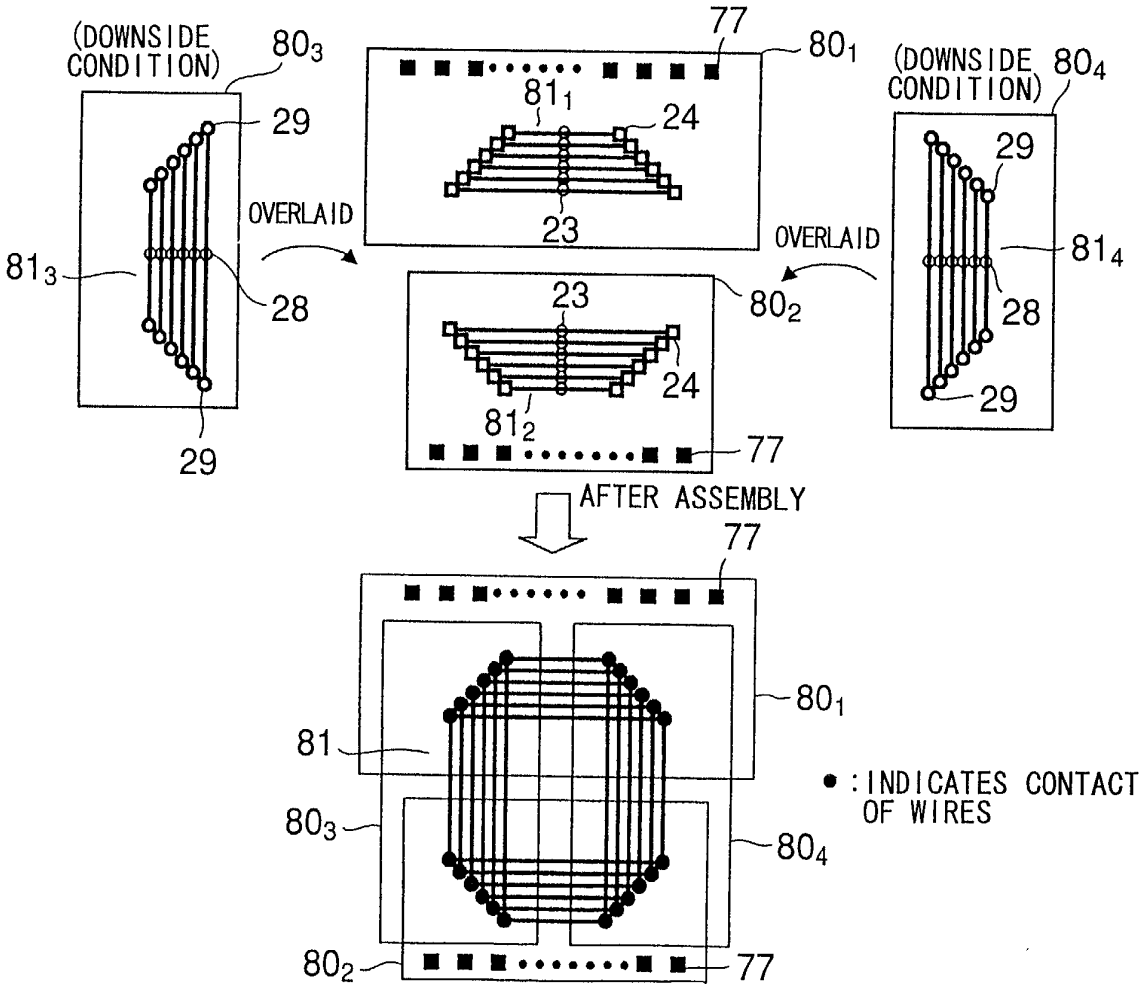

(DOWNSIDE CONDITION)
80₃
29
OVERLAID
81₃
28
29
77
80₁
81₁
24
23
OVERLAID
80₂
23
24
81₂
77
(DOWNSIDE CONDITION)
80₄
29
81₄
28
29
AFTER ASSEMBLY
77
80₁
81
80₃
80₄
80₂
77
● : INDICATES CONTACT OF WIRES

FIG. 33

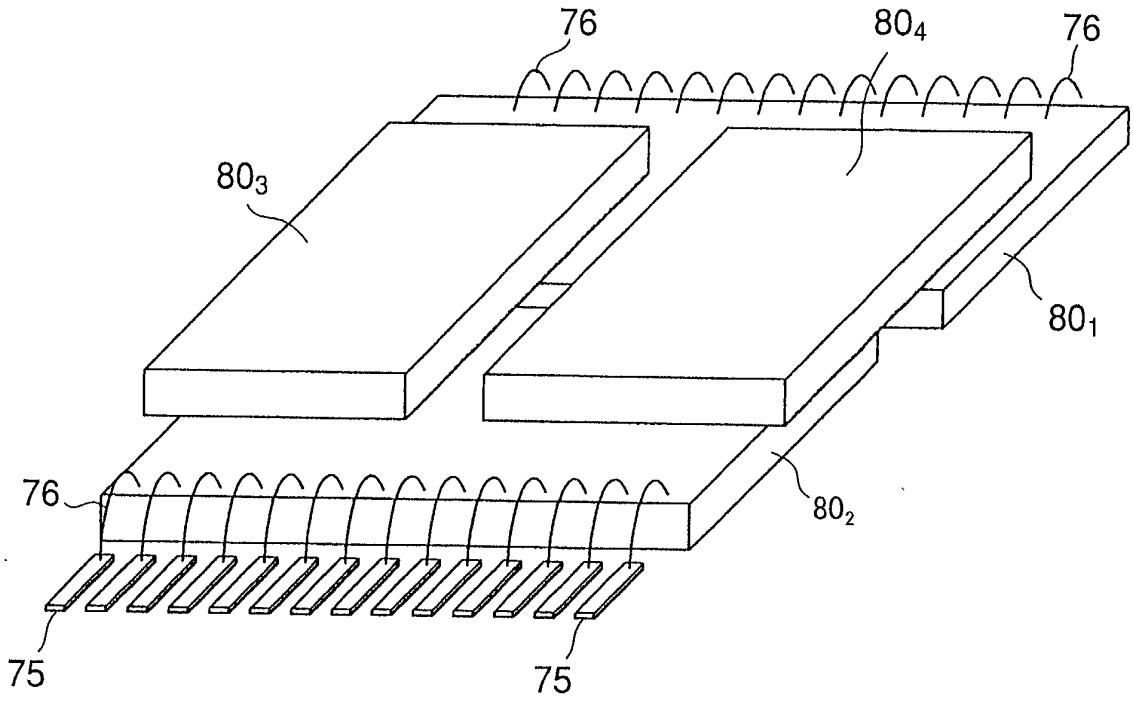
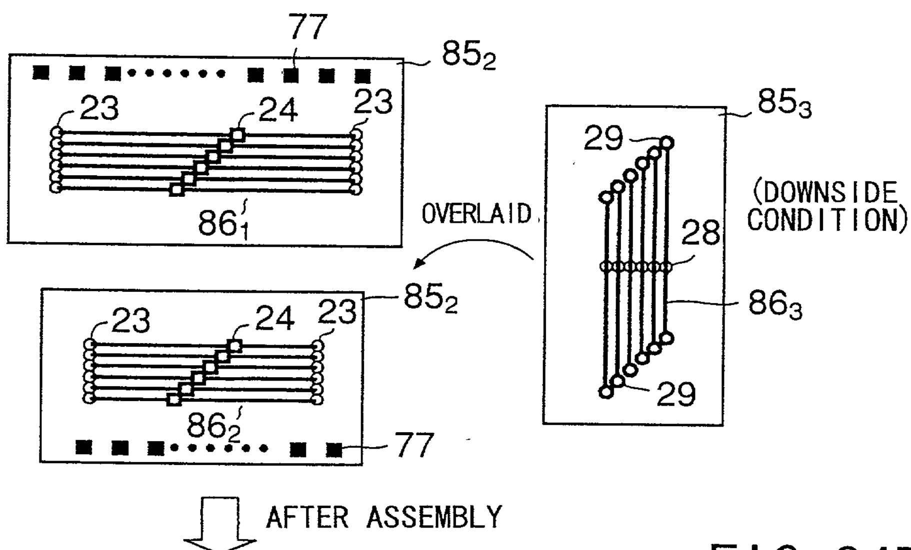


FIG. 34A



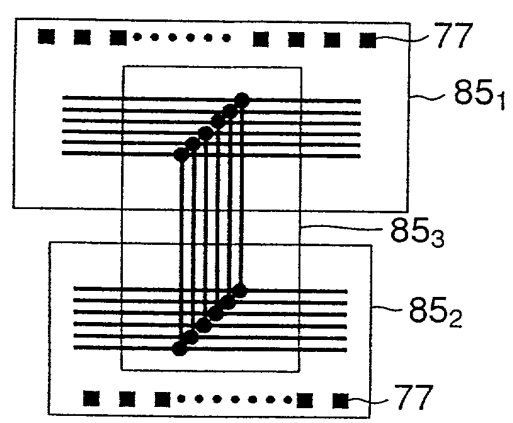


FIG. 34B

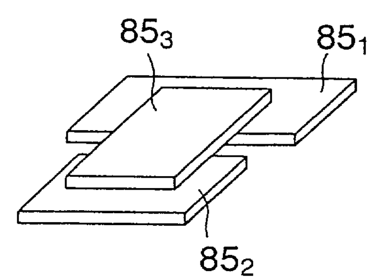


FIG.35

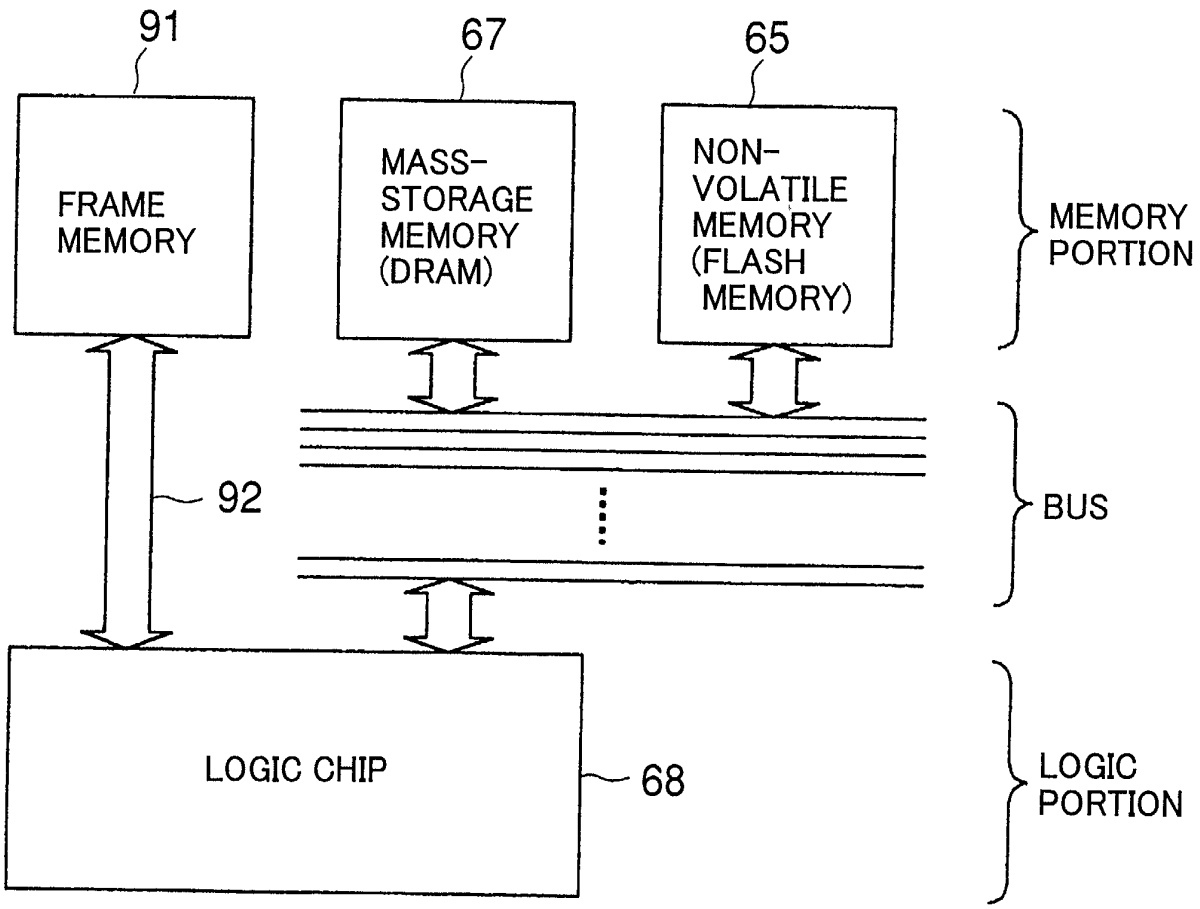

91
67
65
FRAME MEMORY
MASS-STORAGE MEMORY (DRAM)
NON-VOLATILE MEMORY (FLASH MEMORY)
MEMORY PORTION
92
BUS
LOGIC CHIP
68
LOGIC PORTION

FIG. 36

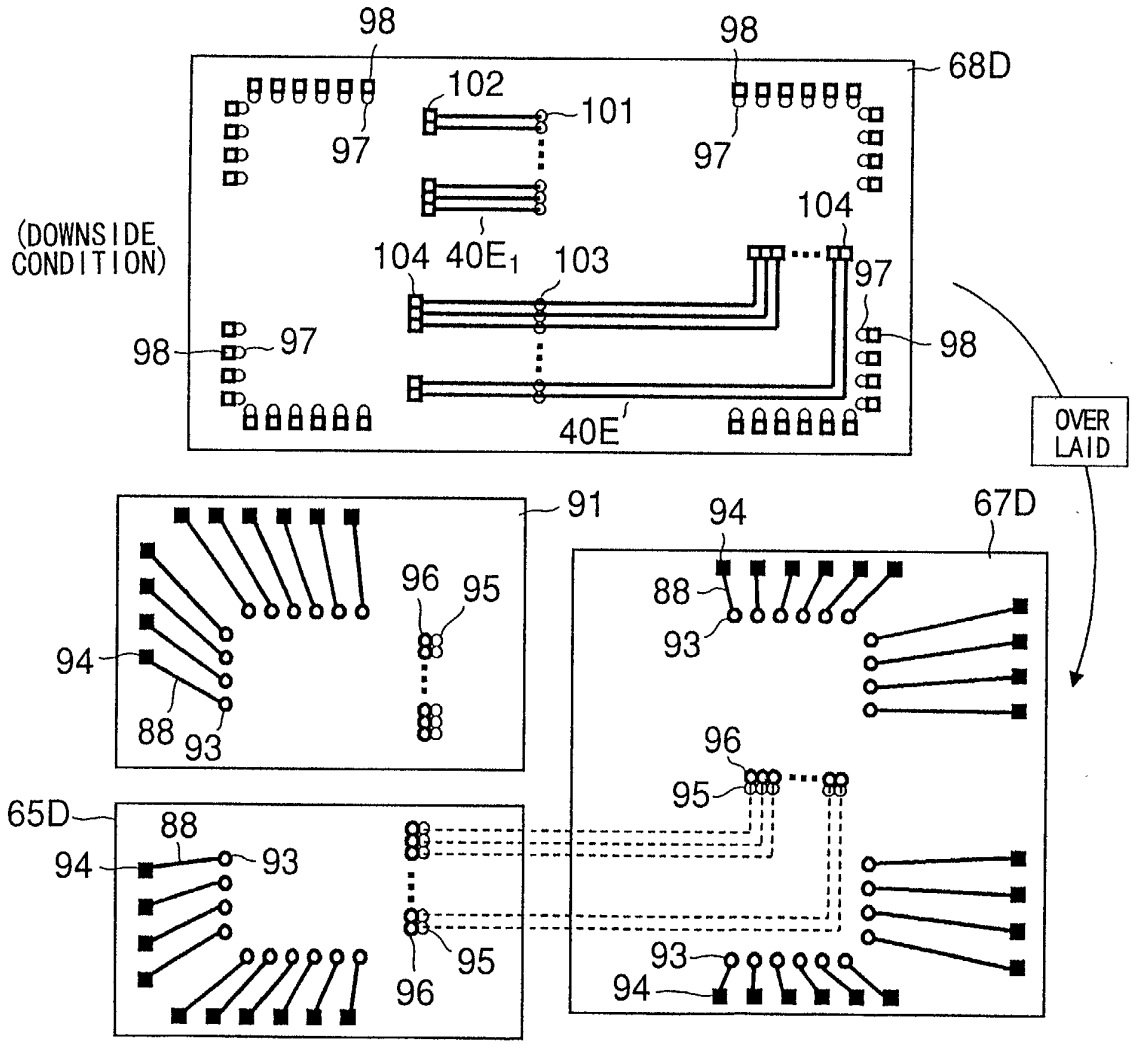

98
98
68D
102
101
97
97
104
(DOWNSIDE CONDITION)
104 40E1 103
97
98
97
98
40E
OVER LAID
91
94
67D
96
95
88
93
94
88
93
65D
88
94
93
96
95
93
94

FIG.37

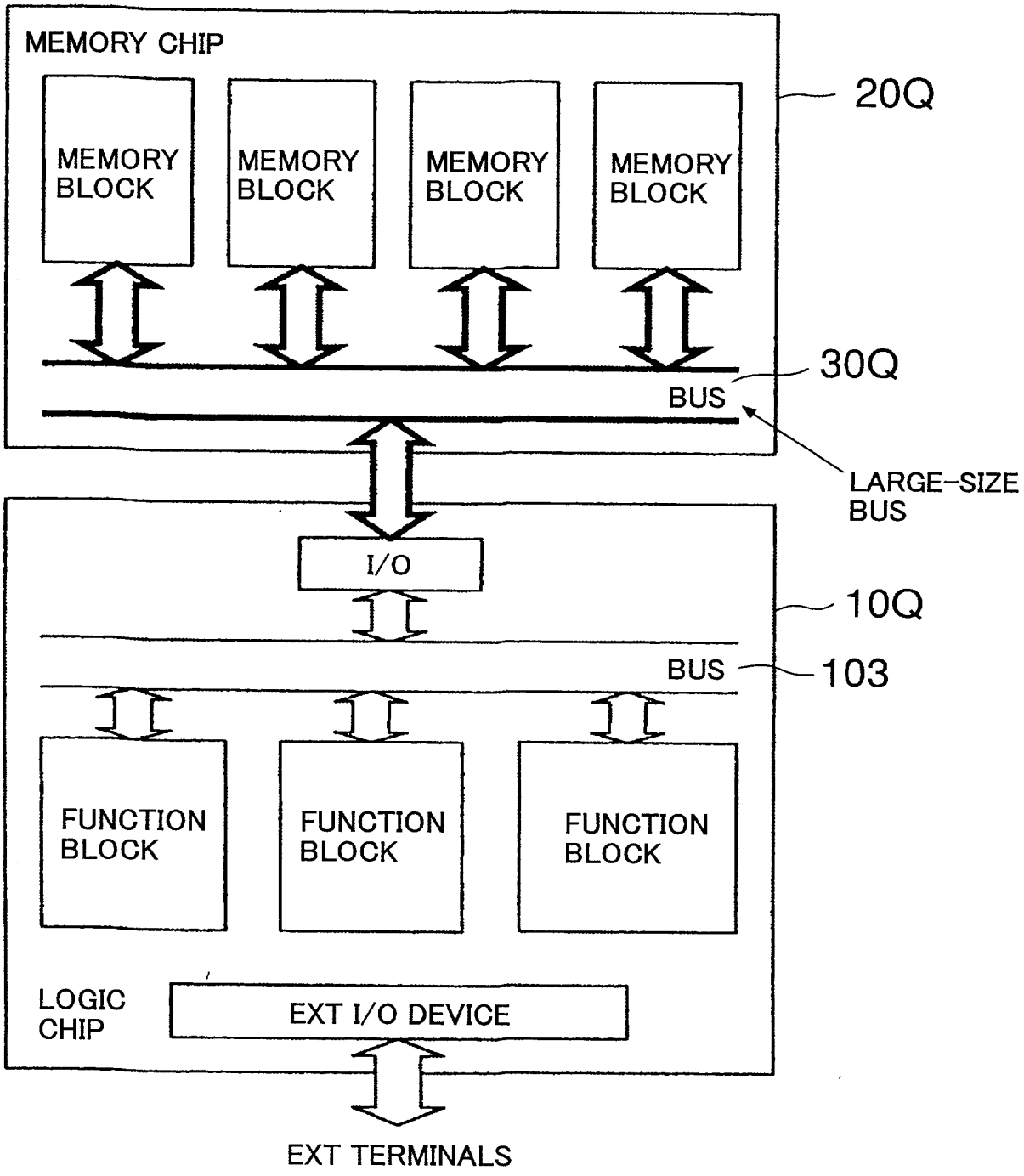

MEMORY CHIP
MEMORY BLOCK
MEMORY BLOCK
MEMORY BLOCK
MEMORY BLOCK
20Q
30Q
BUS
LARGE-SIZE BUS
I/O
10Q
BUS
103
FUNCTION BLOCK
FUNCTION BLOCK
FUNCTION BLOCK
LOGIC CHIP
EXT I/O DEVICE
EXT TERMINALS

FIG.38

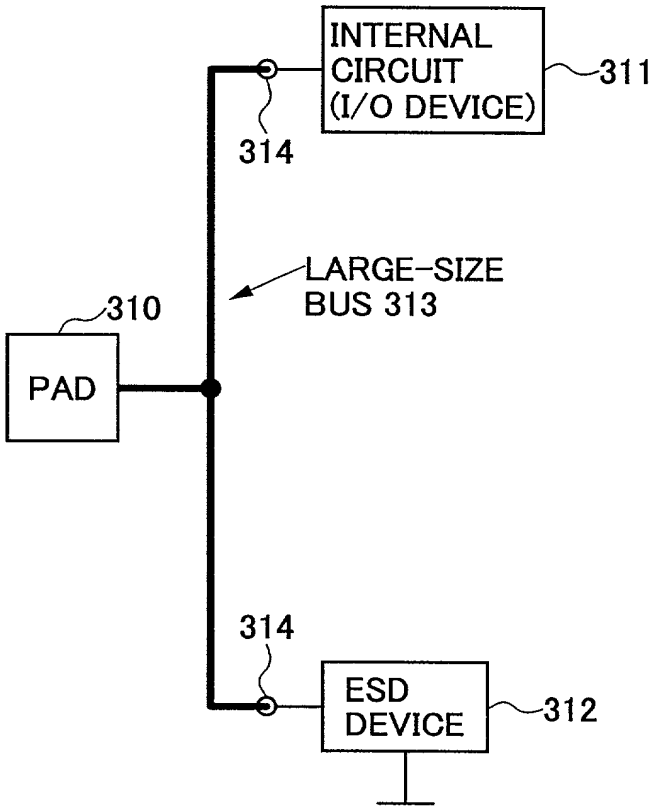


FIG. 39

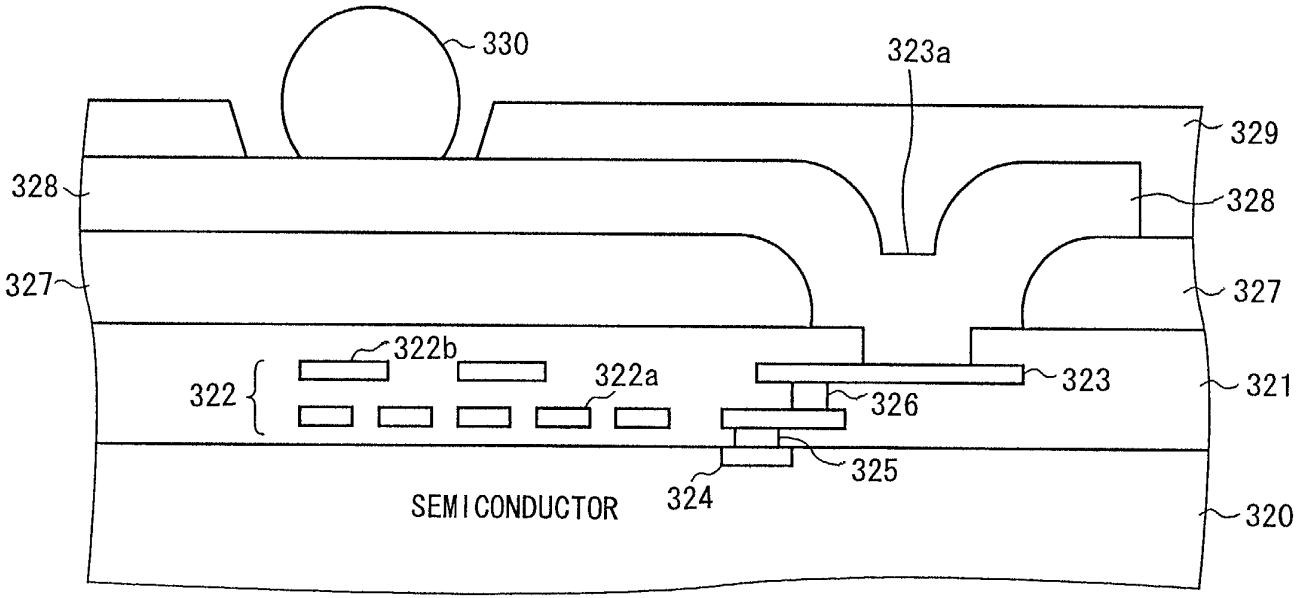

330
323a
329
328
328
327
327
322b
322
322a
323
326
321
325
324
SEMICONDUCTOR
320

FIG.40

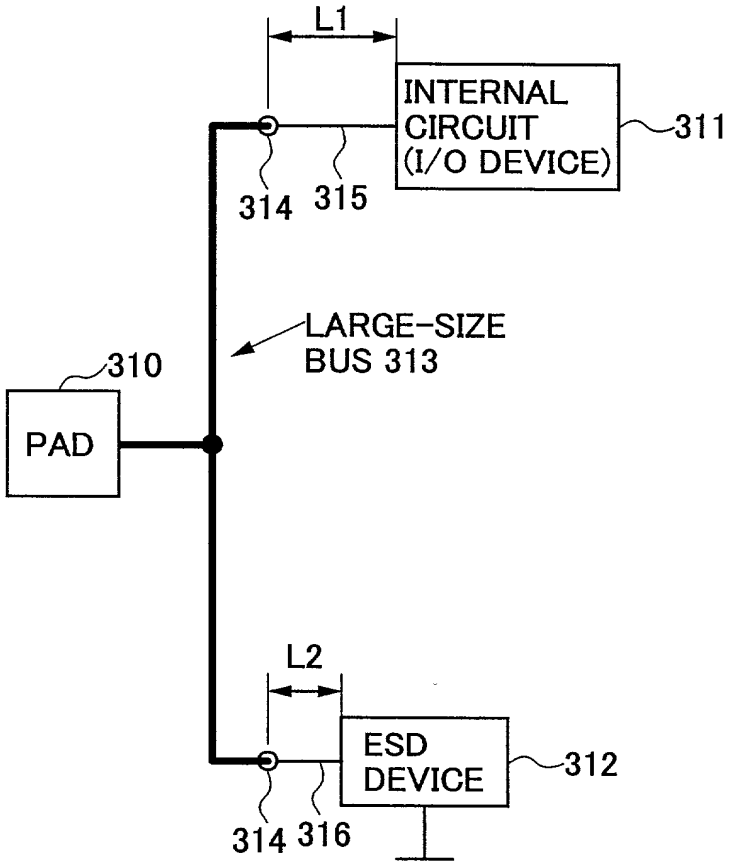

L1
INTERNAL
CIRCUIT
(I/O DEVICE)
311
314
315
LARGE-SIZE
BUS 313
310
PAD
L2
ESD
DEVICE
312
314
316

FIG.41

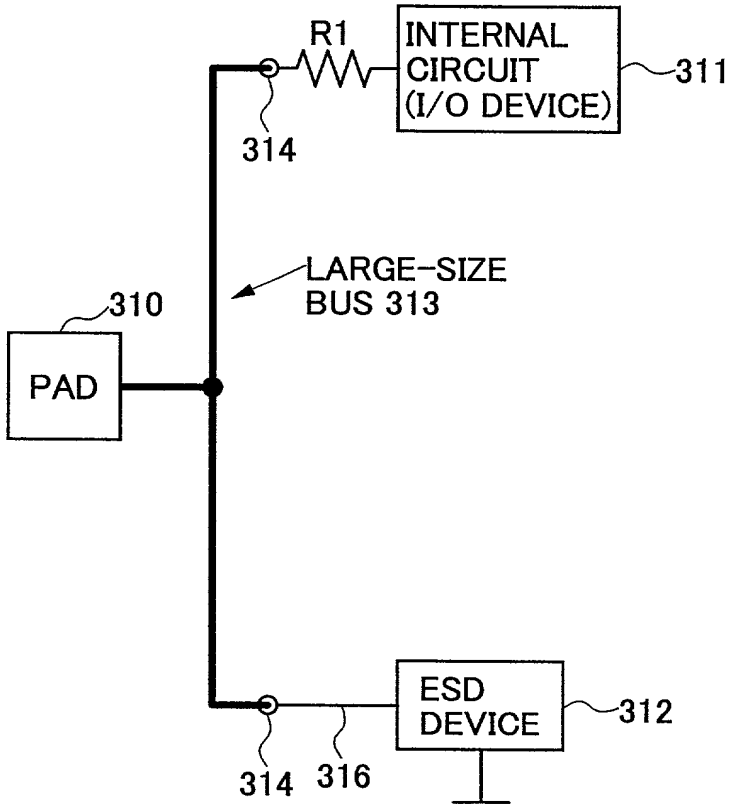


FIG.42

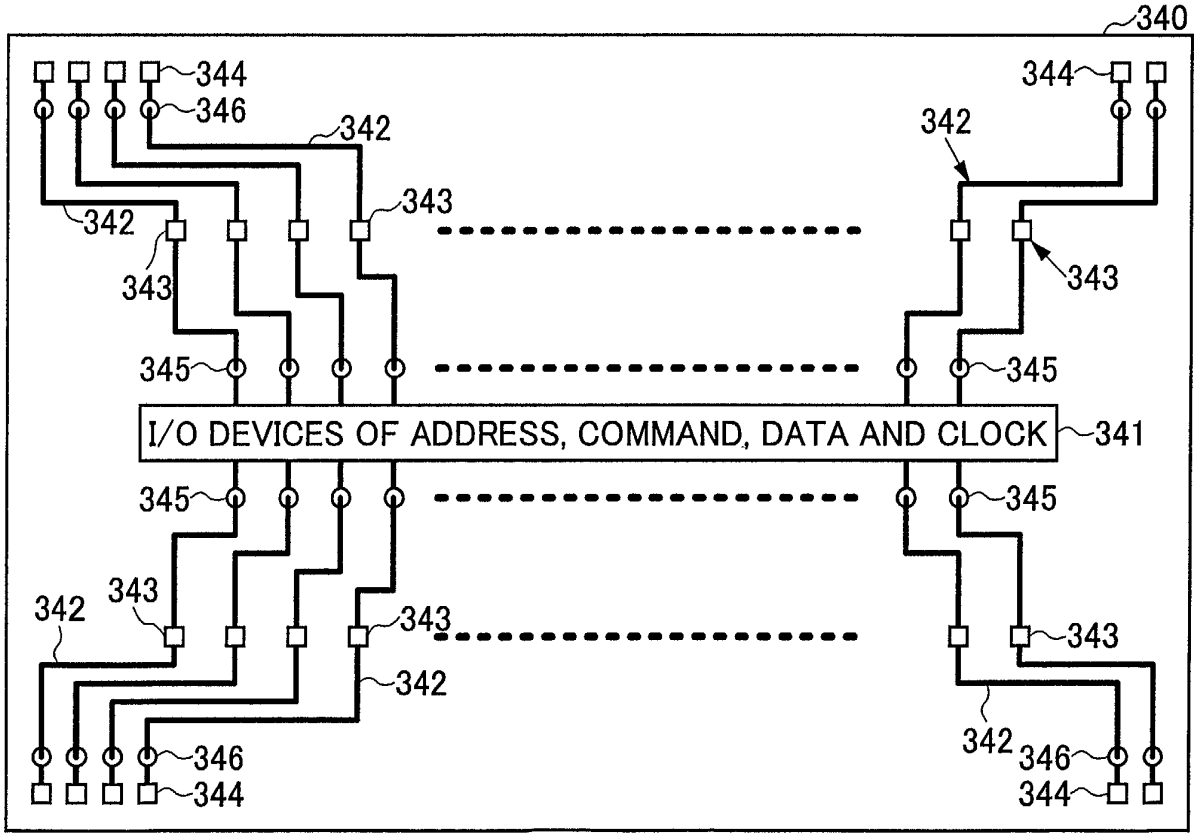

340
344
346
342
343
345
I/O DEVICES OF ADDRESS, COMMAND, DATA AND CLOCK
341

FIG.43

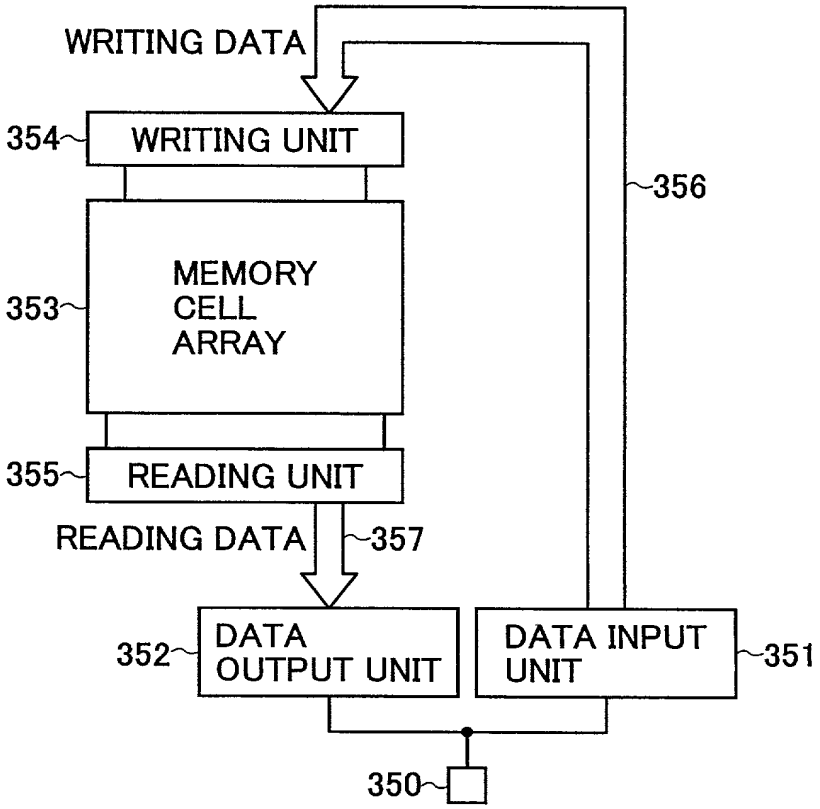

WRITING DATA
354
WRITING UNIT
356
MEMORY
CELL
ARRAY
353
355
READING UNIT
READING DATA
357
352
DATA
OUTPUT UNIT
DATA INPUT
UNIT
351
350

FIG.44A

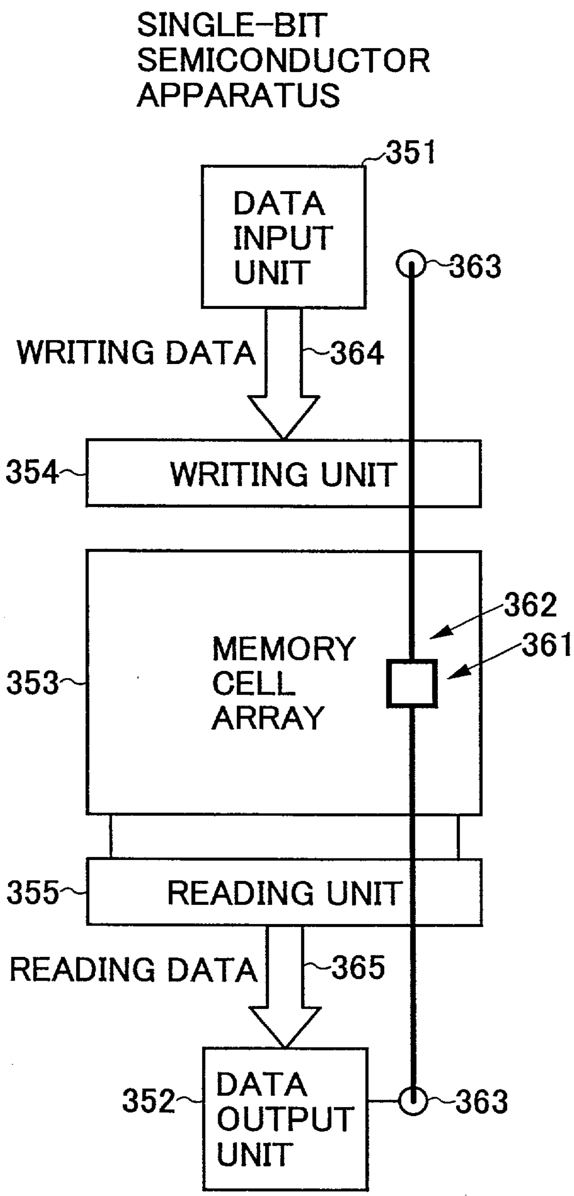


FIG.44B